

MODEL NAME : *AAM00*

PCB NO : *LA-C361P*

BOM P/N :

Dell/Compal Confidential

Schematic Document

SKYLAKE-H

2014-05-22

Rev: 0.0 (M00)

@ : Nopop Component

CONN@ : Connector Component

R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB

TPM@ : TPM function

EMC@ : Pop of EMI parts

VRAMS@ : Samsung GDDR5 for GPU

VRAMH@ : Hynix GDDR5 for GPU

VRAMM@ : Micron GDDR5 for GPU

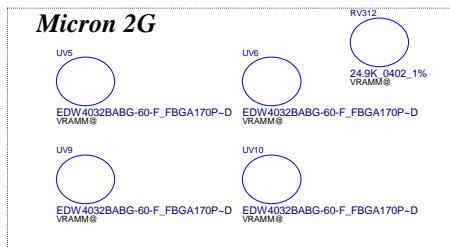
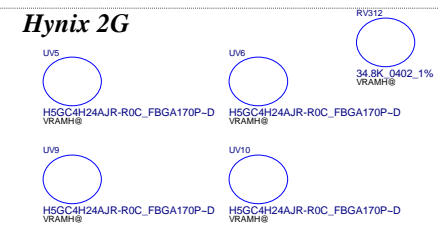
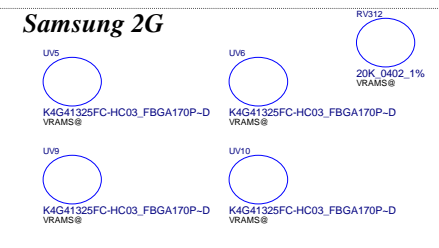
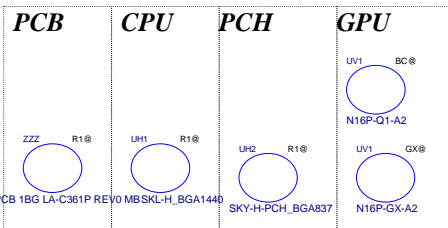
BreakDown@ : for measure power consumption

CSMB@ : CSMB sku

BC@ : BC sku (GPU N16P-Q1)

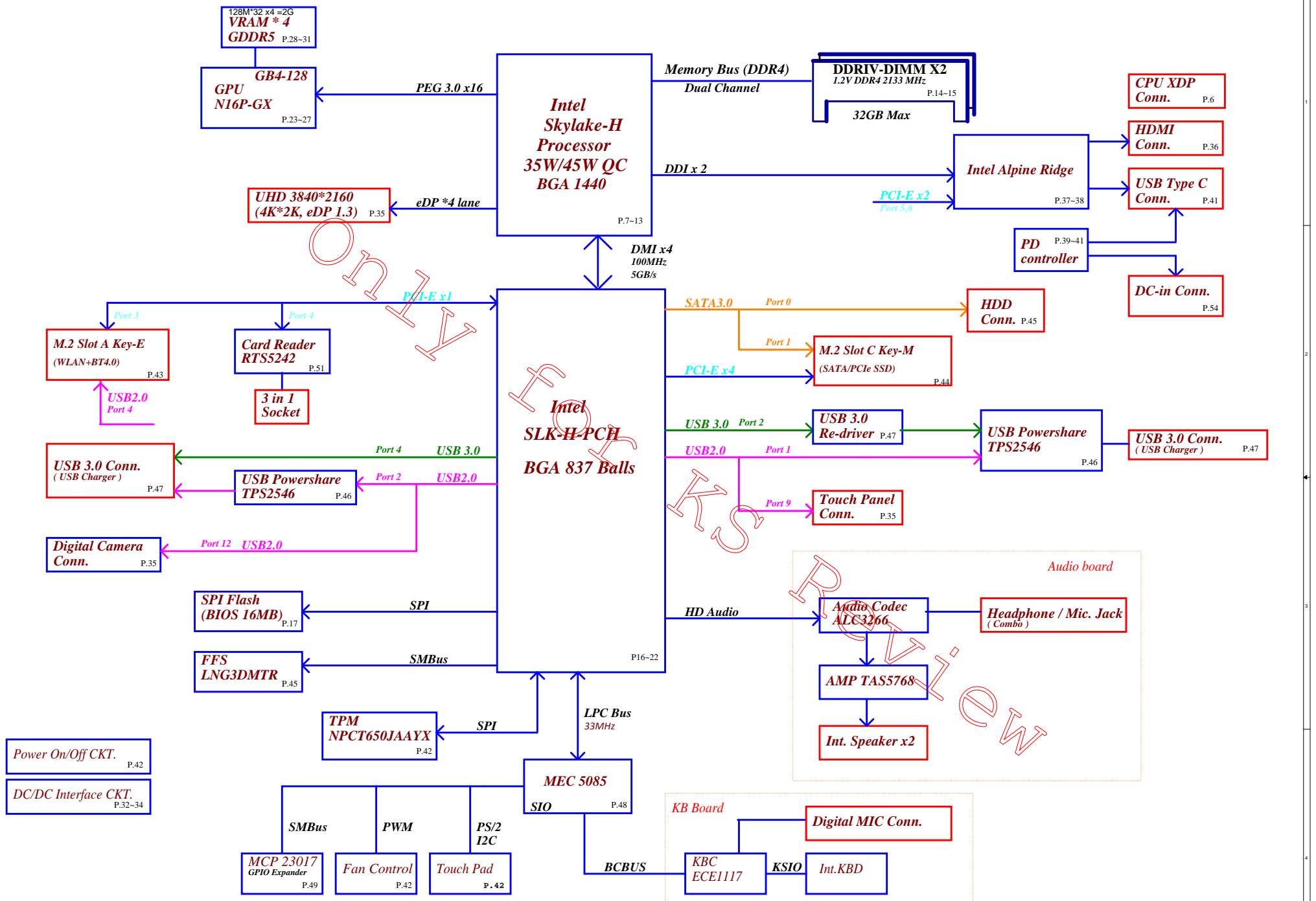
GX@ : GPU N16P-GX

UMA@ / DIS@ : UMA/DIS

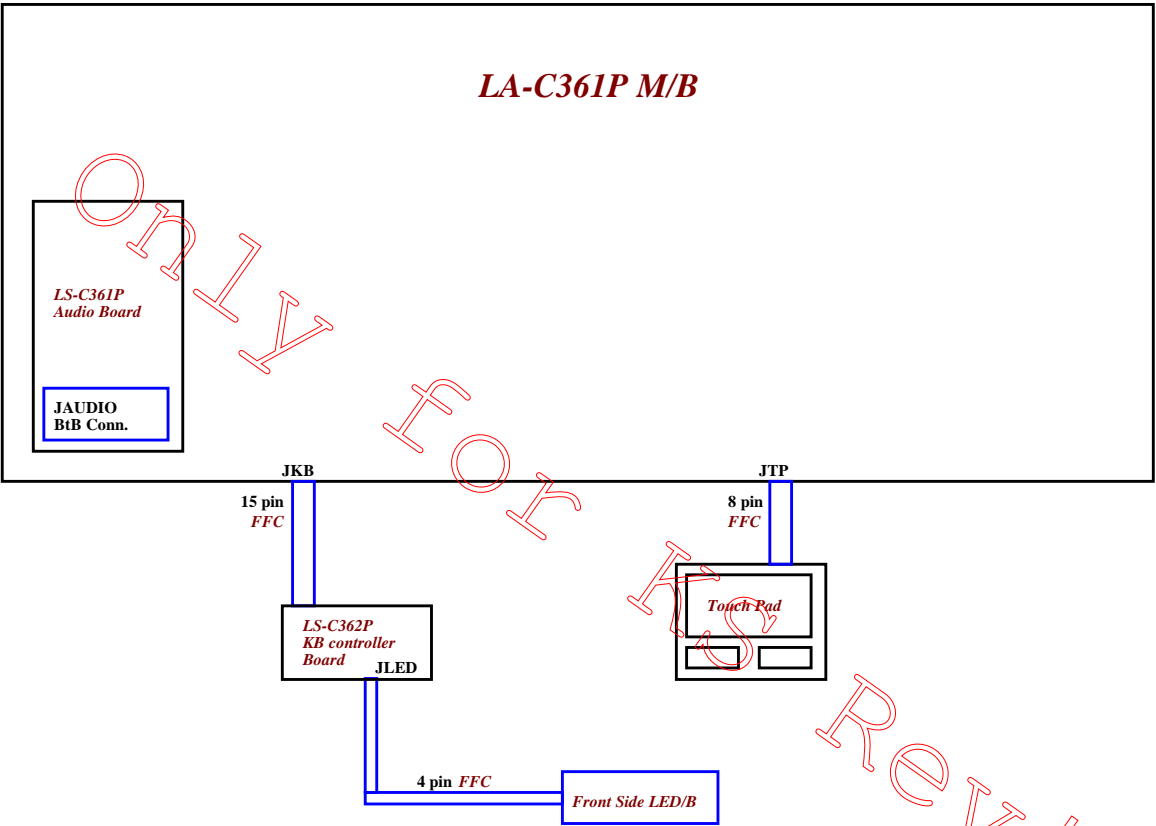


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Board ID	Resistor
X00	N/A
X01	
X02	
X03	
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA



DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

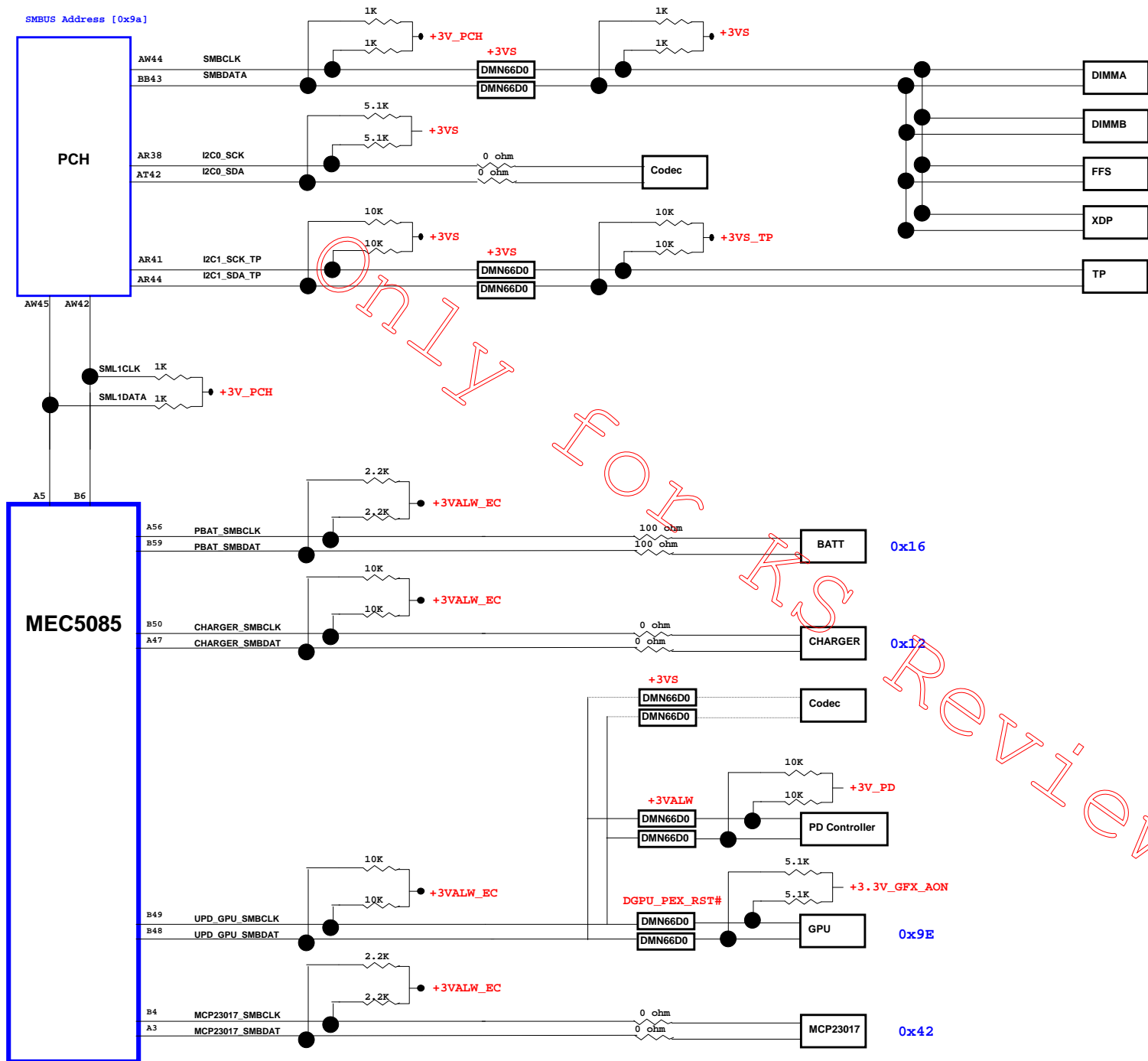
LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

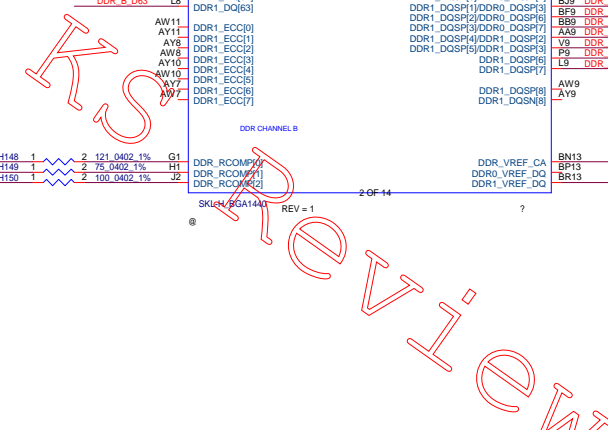
PCI EXPRESS	DESTINATION	USB3	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	CARD READER	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	None		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD	SATA	DESTINATION
Lane 10	SSD	0A	SSD
Lane 11	SSD	1A	N/A
Lane 12	SSD	N/A	N/A
Lane 13	SSD	N/A	N/A
Lane 14	None	0B	None
Lane 15	None	1B	HDD
Lane 16	Alpine Ridge	2	None
		3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

Symbol Note :

 : means Digital Ground
  : means Analog Ground

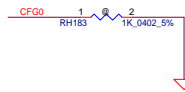




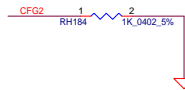
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CFG Straps for Processor

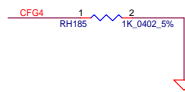
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	<p>* 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>* 0: Lane Reversed</p>



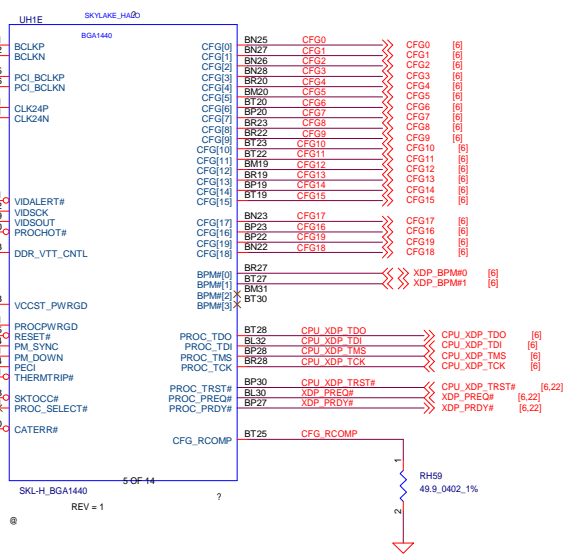
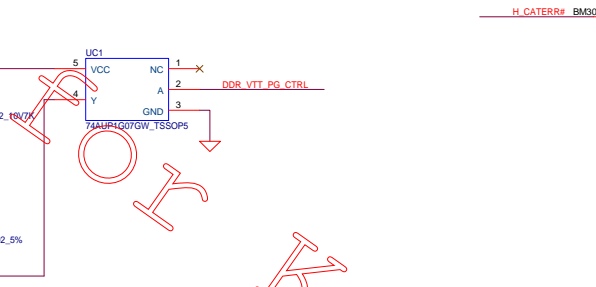
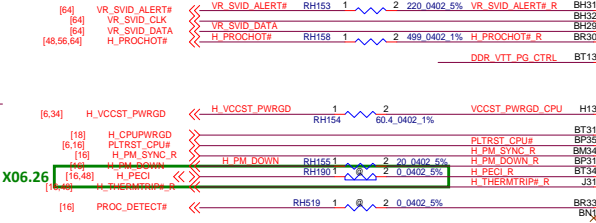
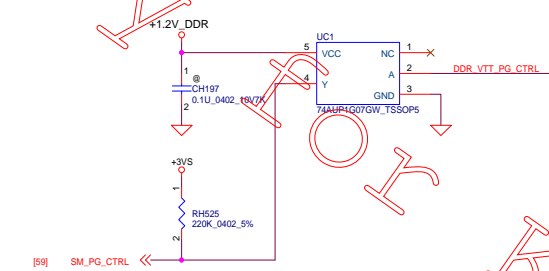
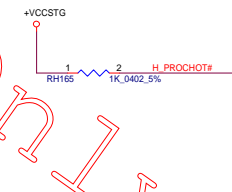
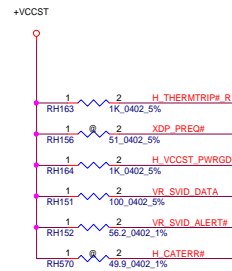
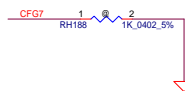
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

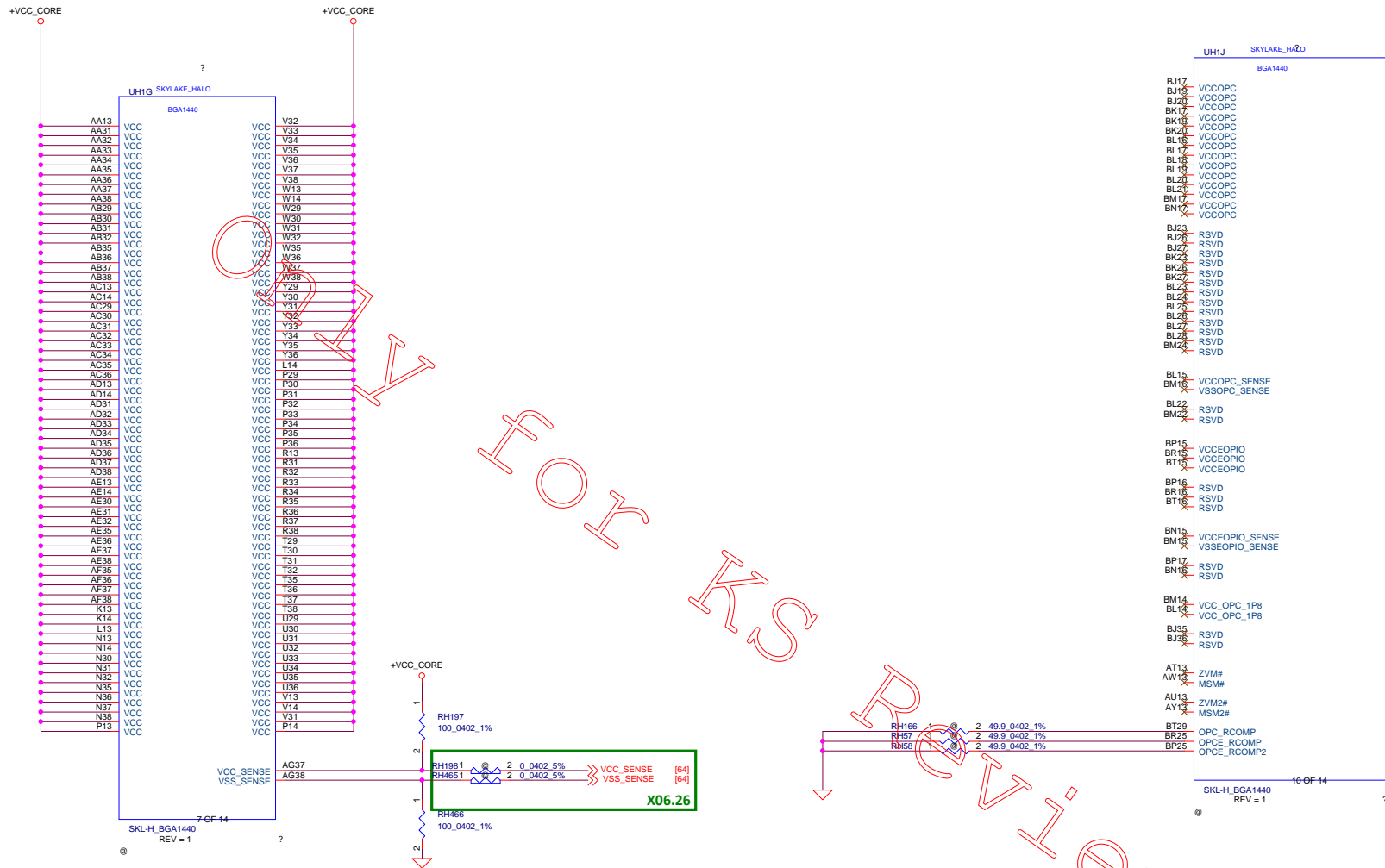


PCIe Port Bifurcation Straps	
CFG[6:5]	<p>* 11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>

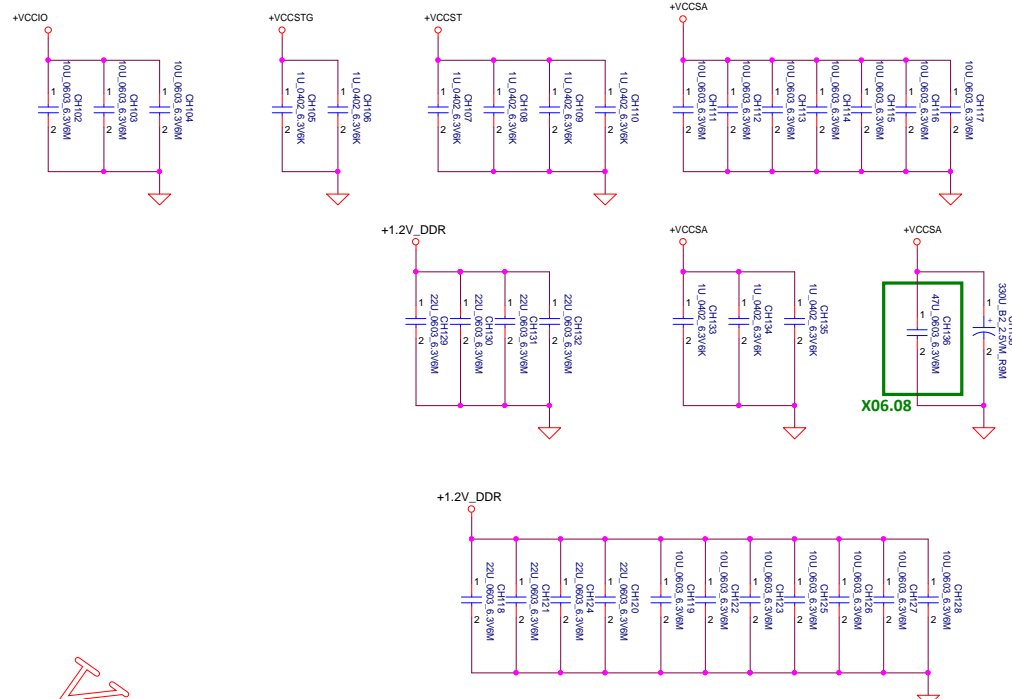


PEG DEFER TRAINING	
CFG7	<p>* 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

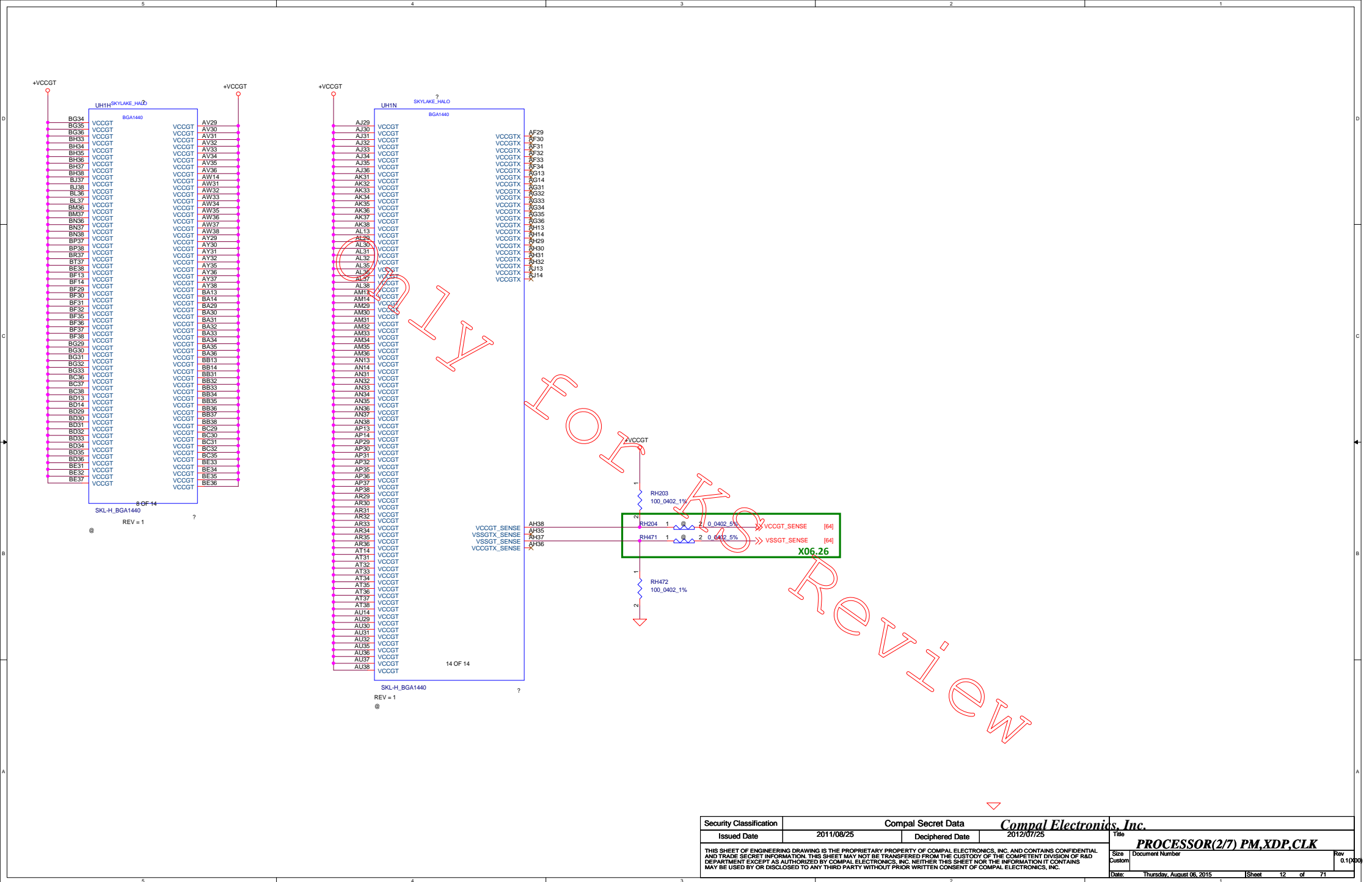




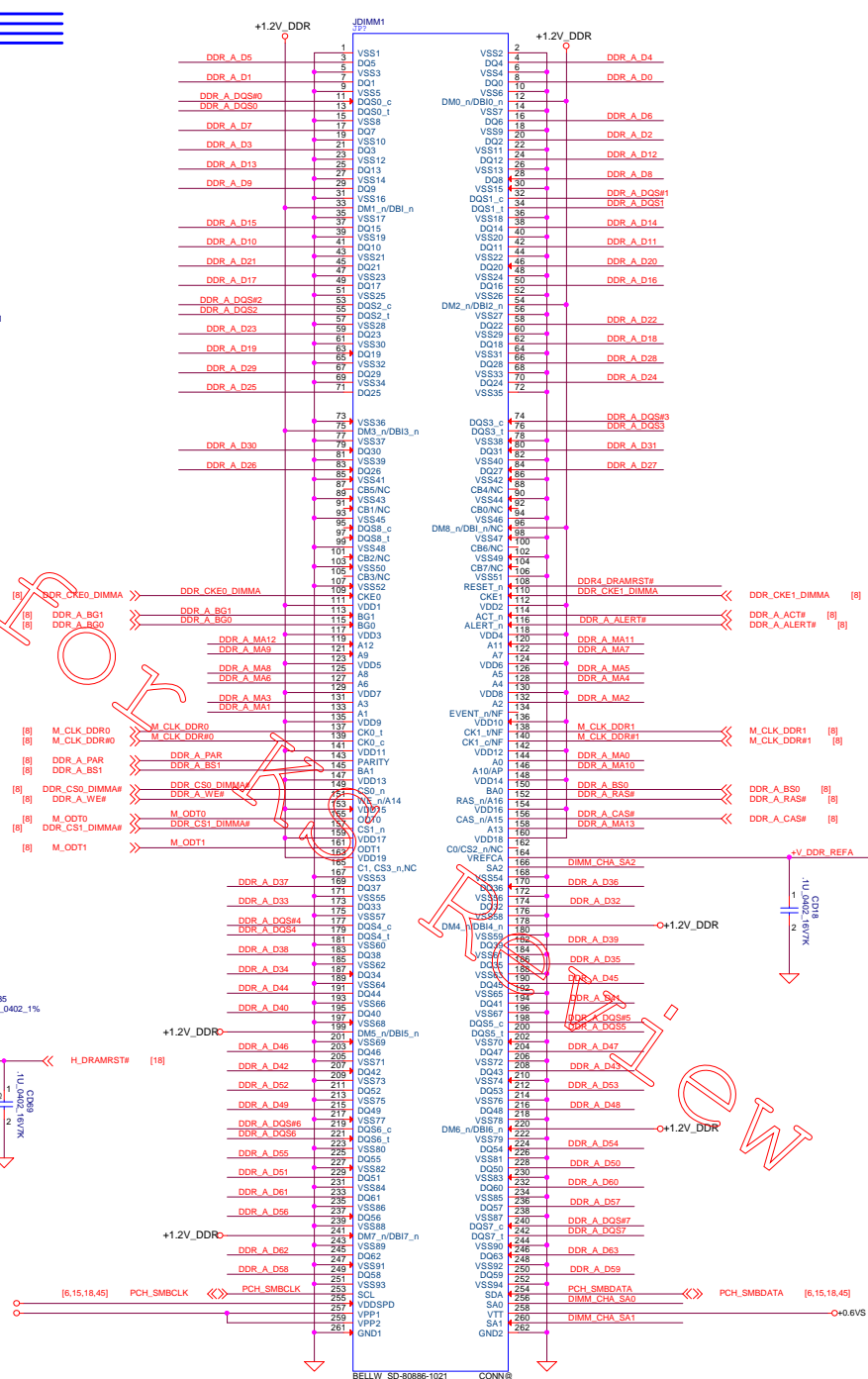
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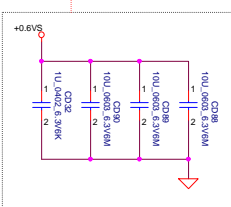


The circuit diagram shows a 5-bit DAC implemented with a 0.6V voltage source and five resistors. The resistors are labeled CD12, CD13, CD14, CD15, and CD16, each with a value of 100.0000 and a tolerance of 0.5000M. The resistors are connected in a ladder configuration to the positive terminal of the 0.6V source. The negative terminal of the source is connected to ground, indicated by a triangle symbol.

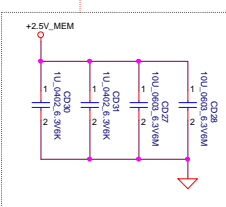


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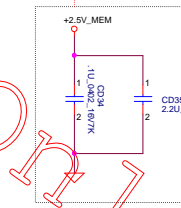
Layout Note:
Place near JDIMM1.258



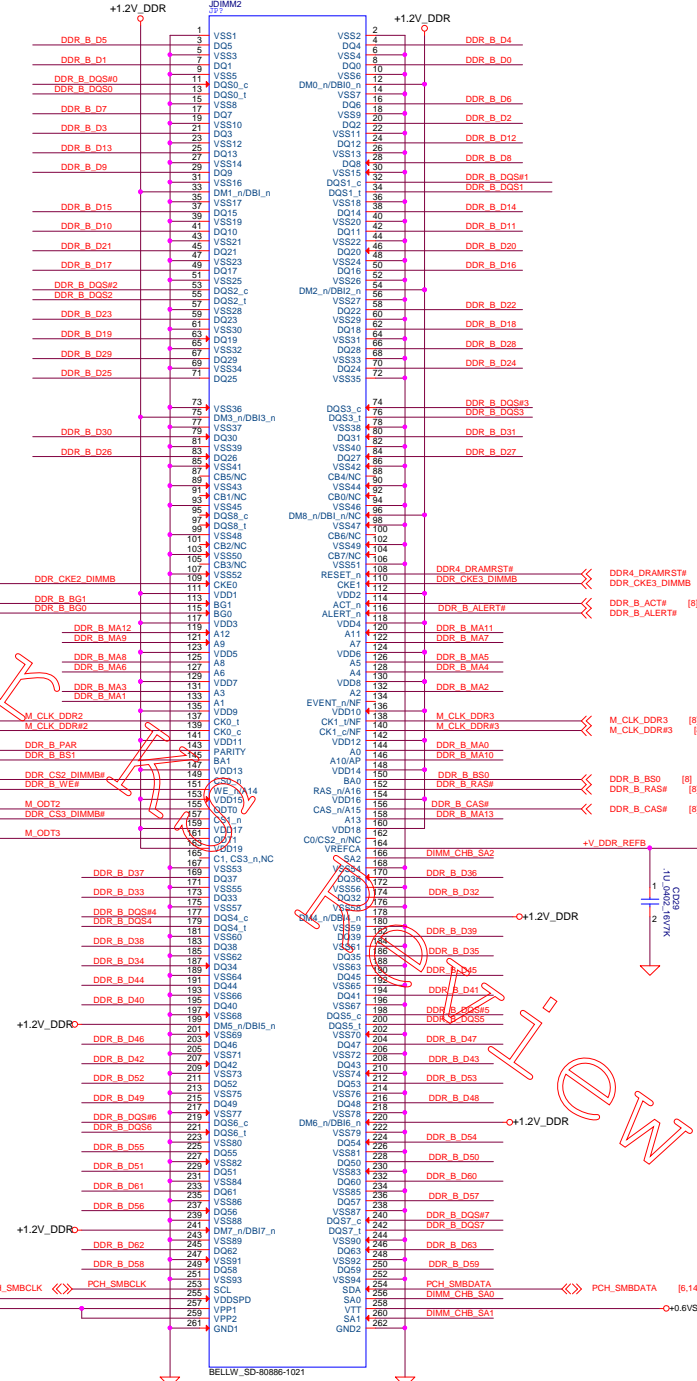
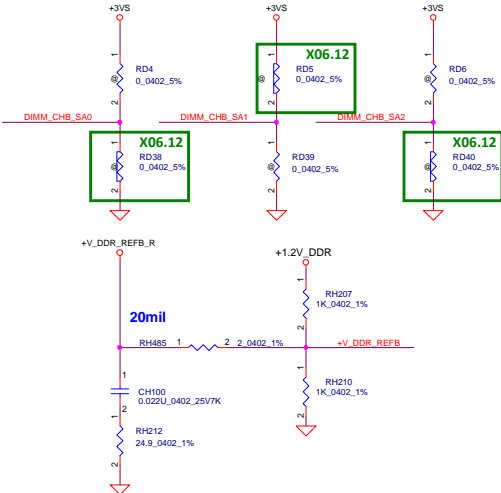
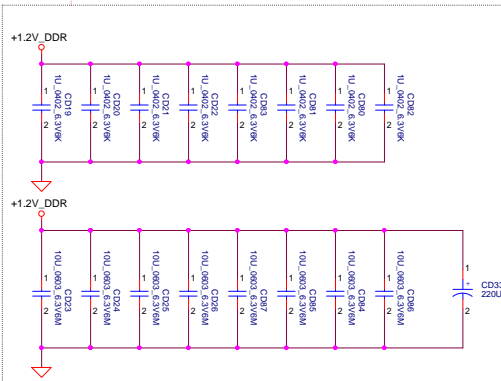
Layout Note:
Place near JDIMM2.257,259



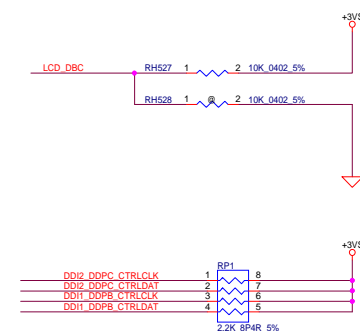
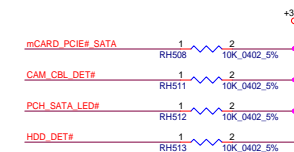
Layout Note:
Place near JDIMM2.255

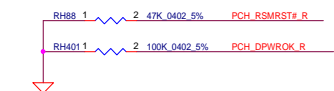
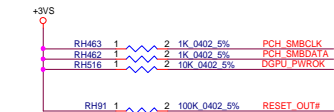
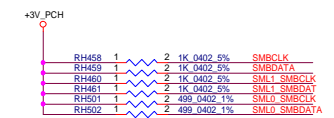
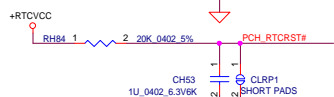
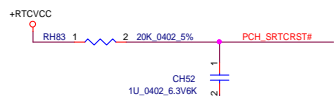


Layout Note:
Place near JDIMMB



All VREF traces should
have 10 mil trace width





[52] HDA_SDOIN0_AUDIO

[7] AUD_AZA_CPU_SDO_R

[7] AUD_AZA_CPU_SDI_R

[7] AUD_AZA_CPU_SCLK_R

[6,48] PCH_RSMRST#

[48] PCH_DPWRCK

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[48] PCH_DPWRCK

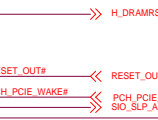
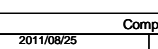
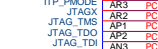
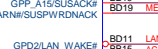
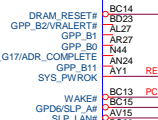
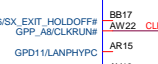
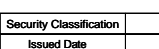
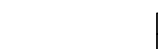
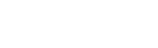
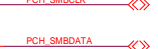
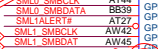
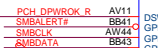
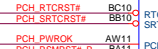
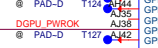
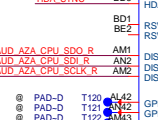
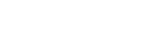
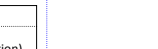
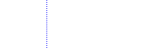
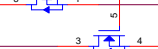
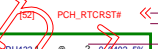
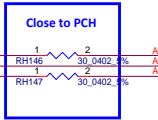
[6,48] PCH_RSMRST#

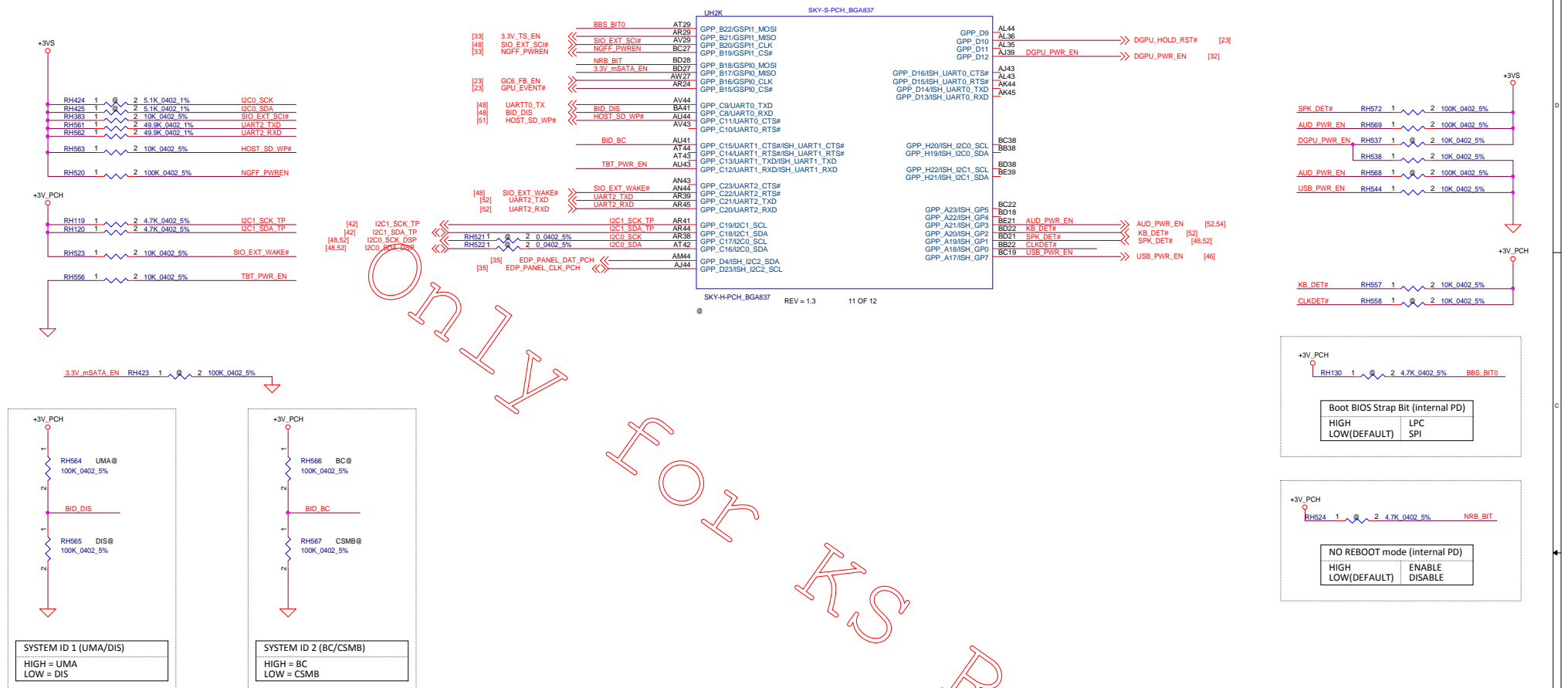
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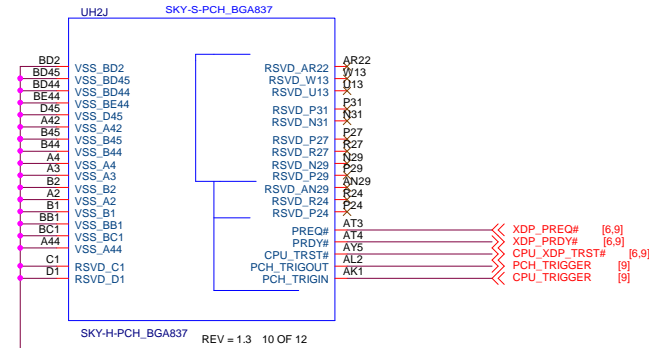
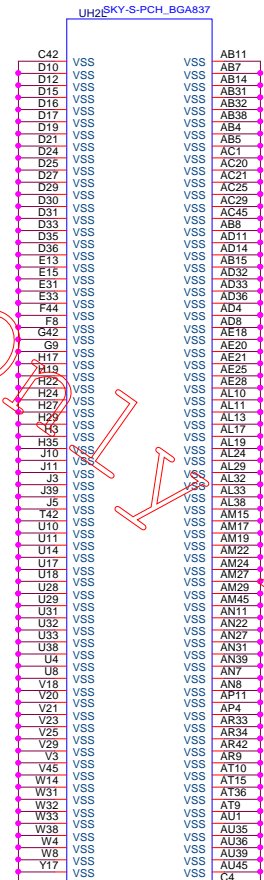
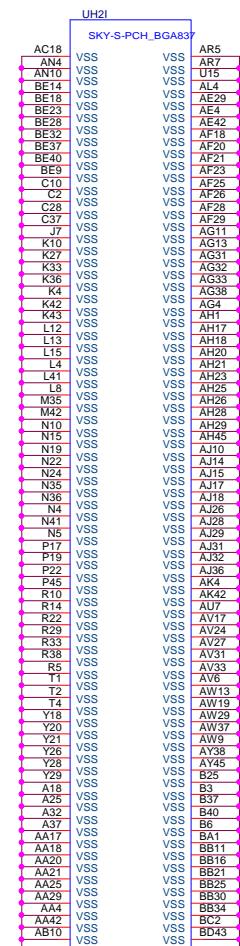
[6,48] PCH_RSMRST#

[48] PCH_DPWRCK

[6,48] PCH_RSMRST#

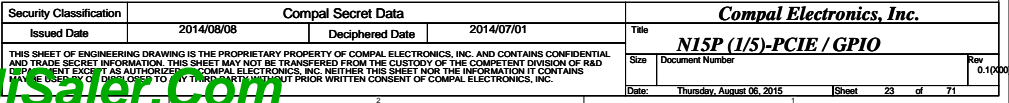


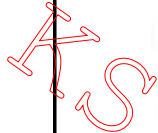




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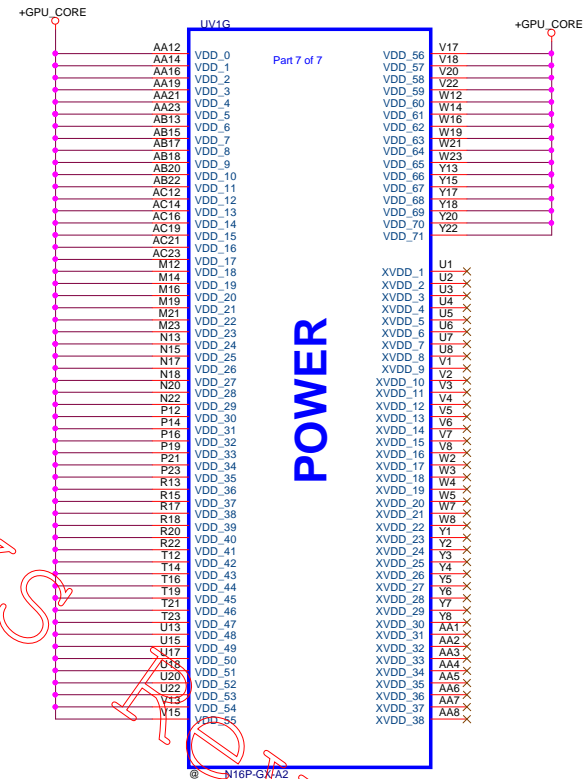
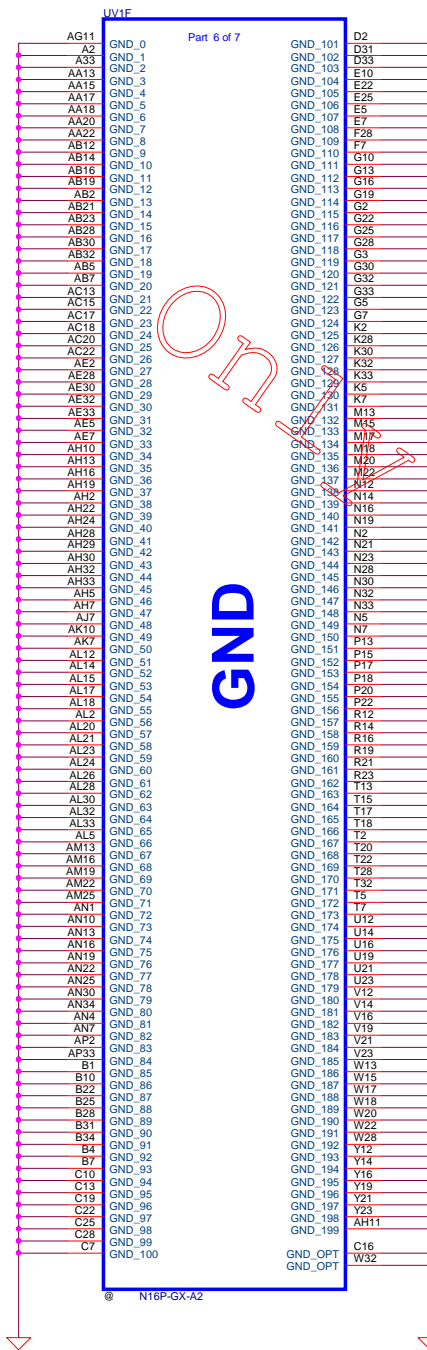
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Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AOH and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AOH and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				



GND

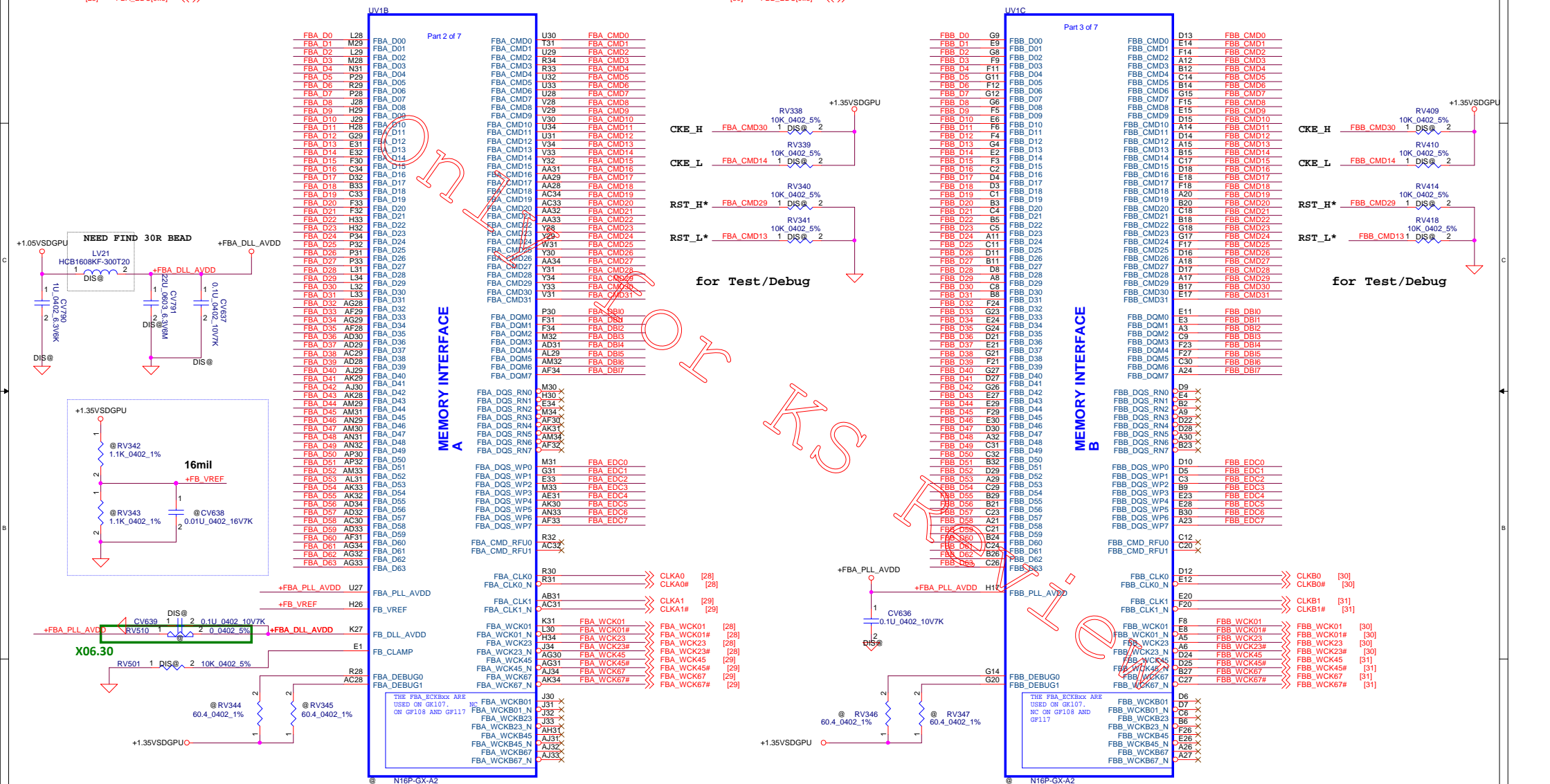
POWER

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				N15P (4/5)-Power / GND			
				Document Number			
				Rev			
				0.1(000)			
Date: Thursday, August 06, 2015				Sheet 26 of 71			

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[28] FBA_D[0..31] <<> FBA_D[0..31]
[29] FBA_D[32..63] <<> FBA_D[32..63]
[28,29] FBA_CMD[0..31] <<> FBA_CMD[0..31]
[29] FBA_DB[4..7] <<> FBA_DB[4..7]
[28] FBA_DB[0..3] <<> FBA_DB[0..3]
[29] FBA_EDC[4..7] <<> FBA_EDC[4..7]
[28] FBA_EDC[0..3] <<> FBA_EDC[0..3]

[30] FBB_D[0..31] <<> FBB_D[0..31]
[31] FBB_D[32..63] <<> FBB_D[32..63]
[30,31] FBB_CMD[0..31] <<> FBB_CMD[0..31]
[31] FBB_DB[4..7] <<> FBB_DB[4..7]
[30] FBB_DB[0..3] <<> FBB_DB[0..3]
[31] FBB_EDC[4..7] <<> FBB_EDC[4..7]
[30] FBB_EDC[0..3] <<> FBB_EDC[0..3]



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Date: Thursday, August 06, 2015				Sheet	27 of 71

Memory Partition A - Lower 32 bits

64X32 GDDR5

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0...31	GB2-64, GB4-128	Channel 1 32...63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA3	CMD19	A4_BA3
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	R5T*	CMD29	R5T*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

CLKA0# 1 DIS@ 2 CLKA0# 80.6_0402_1% [27] CLKA0# CLKA0# [27]

FBA EDC0 C2
FBA EDC1 C13
FBA EDC2 R13
FBA EDC3 R2

FBA DBI0 D2
FBA DBI1 D13
FBA DBI2 P13
FBA DBI3 P2

CLKA0 J12
CLKA0# J11
FBA_CMD14 J3

FBA_CMD9 J5
FBA_CMD6 K4
FBA_CMD7 K5
FBA_CMD4 K10
FBA_CMD3 K11

FBA_CMD1 H10
FBA_CMD2 H11
FBA_CMD11 H5
FBA_CMD10 H4

A5
U5

RV352 1 DIS@ 2 1K 0402 1%
RV353 1 DIS@ 2 1K 0402 1%
RV354 1 DIS@ 2 121 0402 1%

FBA_CMD8 J4
FBA_CMD12 G3
FBA_CMD10 G12
FBA_CMD15 L3
FBA_CMD5 L12

FBA_WCK01# D5
FBA_WCK01 D4
FBA_WCK23# P5
FBA_WCK23 P4

FBA_CMD13 J2

WCK01#
WCK01
WCK23#
WCK23
WCK01#
WCK01

VREFD
VREFD
VREFC

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

RESET#

SGRAM GDDR5

H5GC4H24AJR-R0C
K4G41325FC-HC03
EDW4032BABG-60-F

K4G41325FC-HC04_FBA170-D

Security Classification

Compal Secret Data

Issued Date

2014/08/08

Deciphered Date

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VRAM GDDR5 A Lower

Size Document Number Rev 0.1(00)

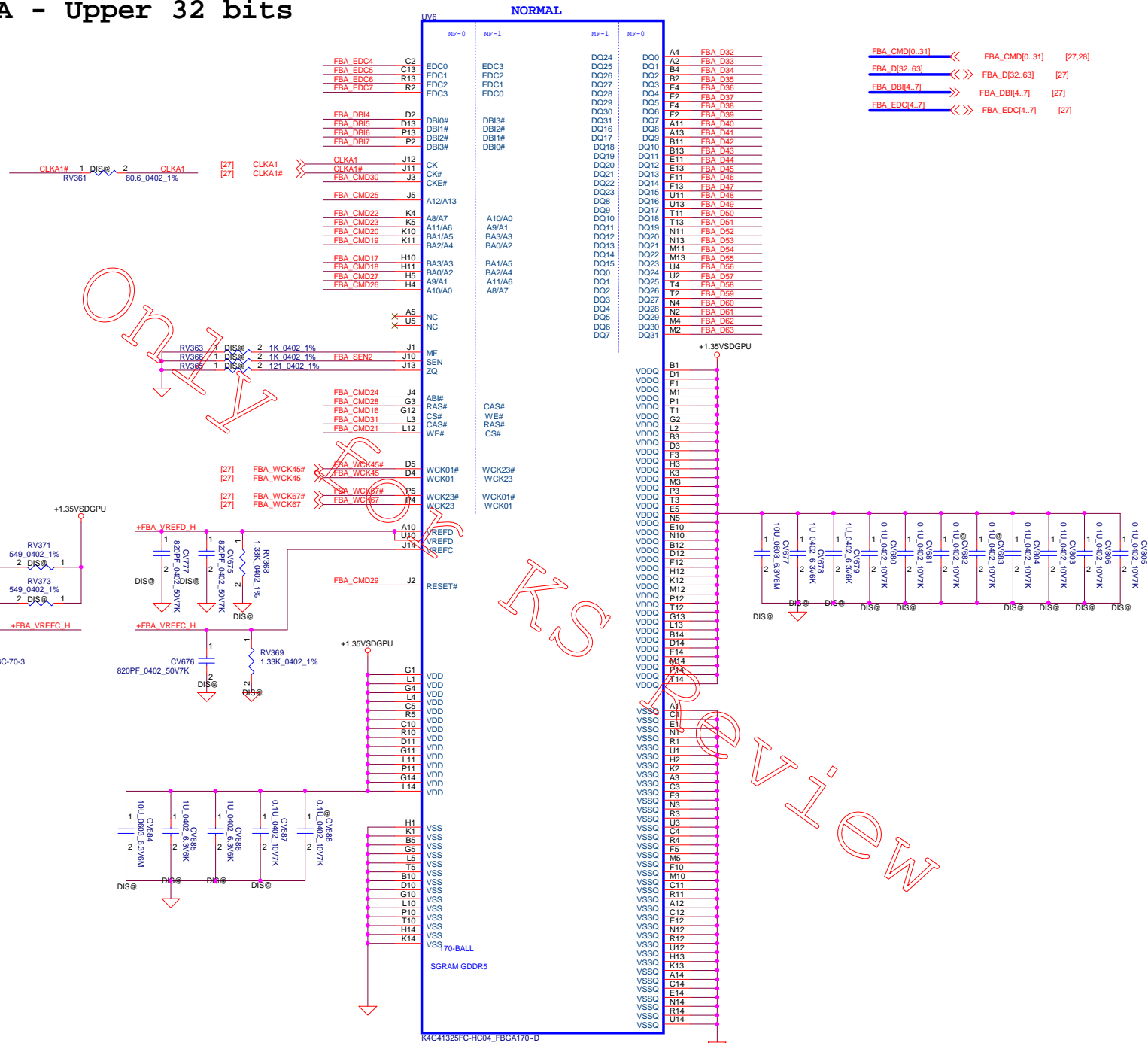
Date: Thursday, August 06, 2015 Sheet 28 of 71

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Memory Partition A - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_AB	CMD22	A7_AB
CMD7	A8_A11	CMD23	A8_A11
CMD8	AB*	CMD24	AB*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	R5T*	CMD29	R5T*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



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				Size	Document Number	Rev
				0.1(000)		
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64X32 GDDR5

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB*	CMD24	AB*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



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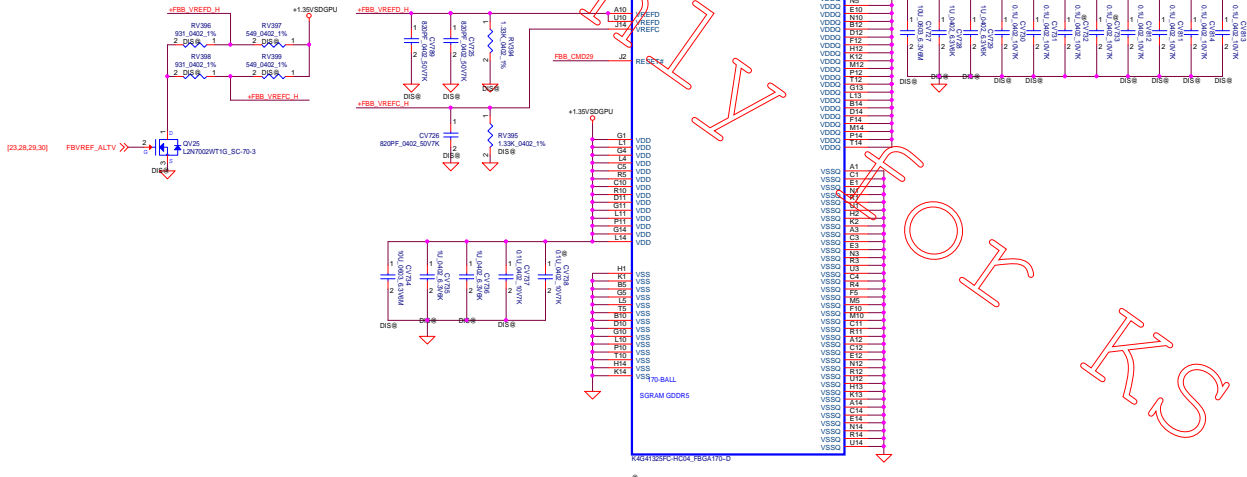
3

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Memory Partition B - Upper 32 bits

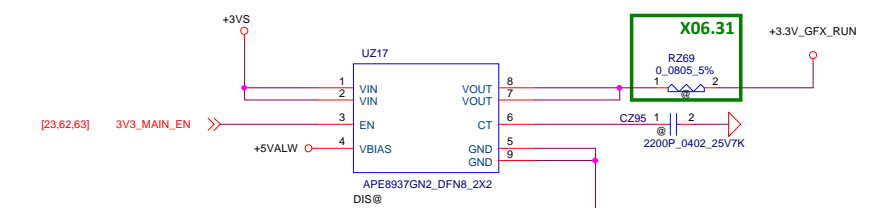
Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128		Channel 0 0, 31	GB2-64, GB4-128		Channel 1 32, 63
CHD0		C5	CHD19		C5
CHD01	A3, B43	CHD17	A3, B43		
CHD02	A2, B40	CHD18	A2, B40		
CHD03	A4, B42	CHD19	A4, B42		
CHD04	A5, B41	CHD20	A5, B41		
CHD05	WE*	CHD1	WE*		
CHD06	A7, A8	CHD22	A7, A8		
CHD07	AB, A11	CHD03	AB, A11		
CHD08	AB*	CHD04	AB*		
CHD09	A12, RFU	CHD05	A12, RFU		
CHD010	A0, A10	CHD06	A0, A10		
CHD011	A1, A9	CHD07	A1, A9		
CHD012	RA*	CHD08	RA*		
CHD013	RS*	CHD09	RS*		
CHD014	CR*	CHD30	CR*		
CHD015	CA*	CHD31	CA*		

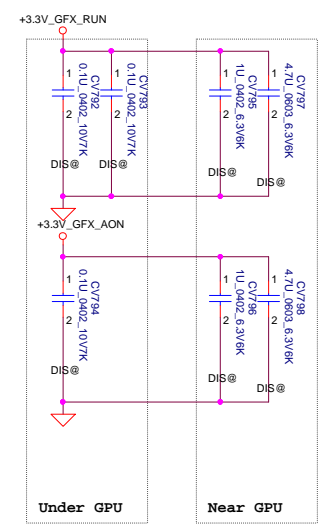
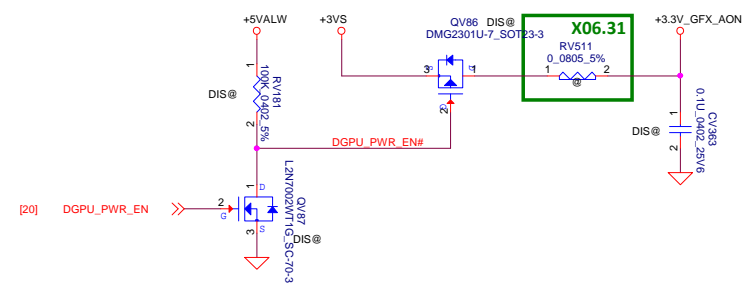


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				VRAM GDDR5 B Upper	
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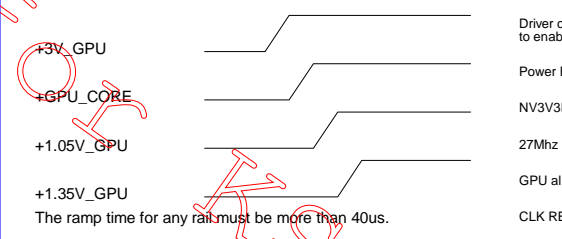
+3.3V_GFX_RUN



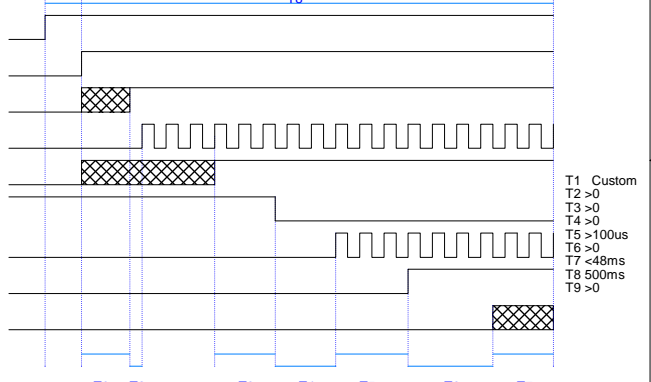
+3VALW to +3.3V_GFX_AON



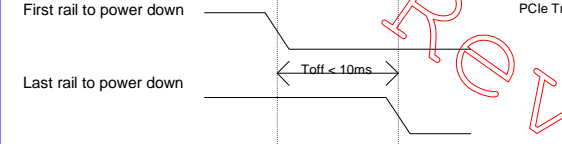
GPU Power Up Power Rail Sequence



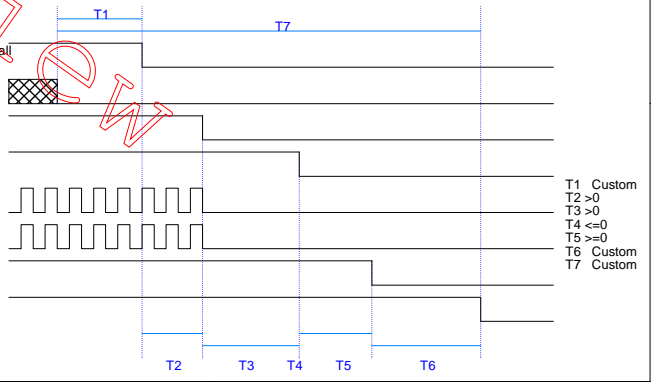
GPU Power Up Sub-system Sequence



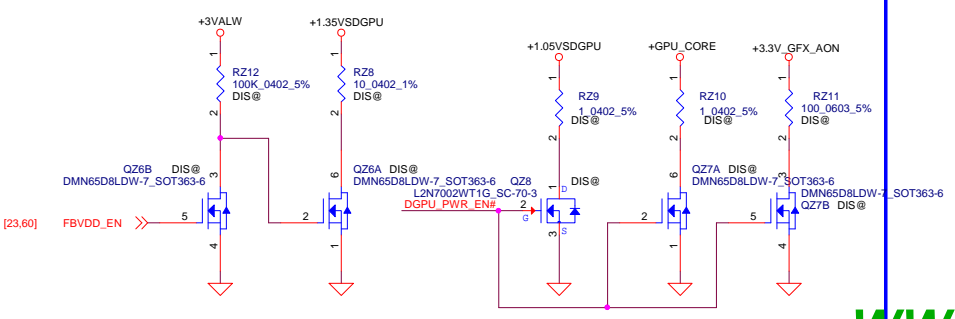
GPU Power Down Sequence



GPU Power Down Sub-system Sequence

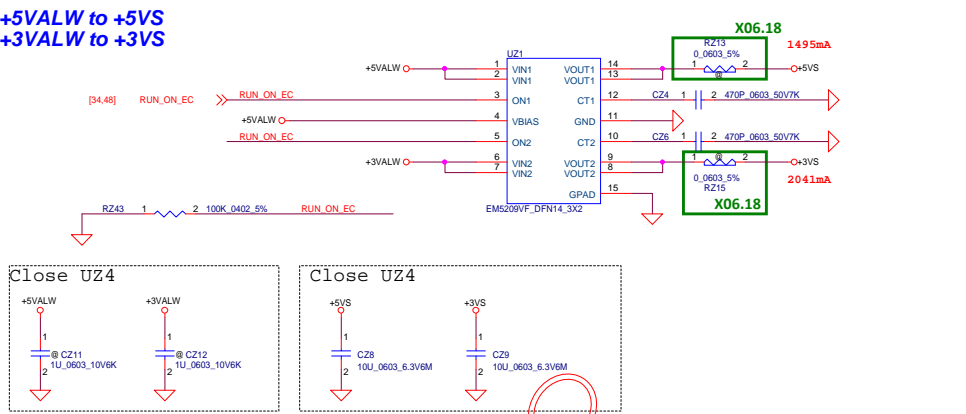


Discharge

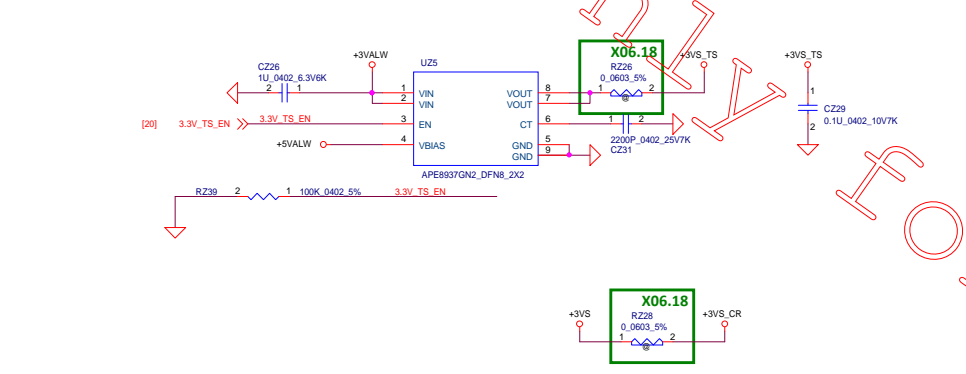


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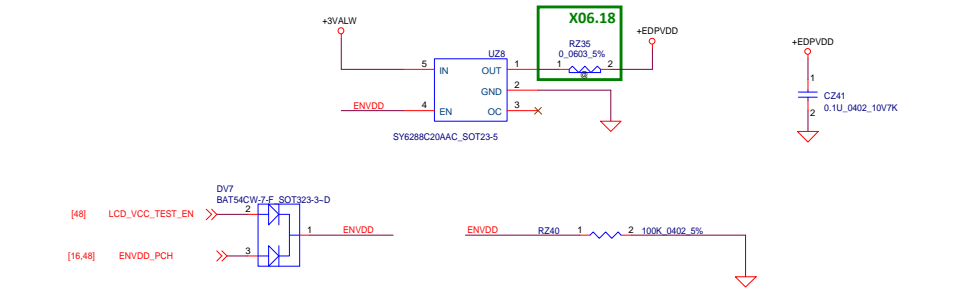
+5VALW to +5VS
+3VALW to +3VS



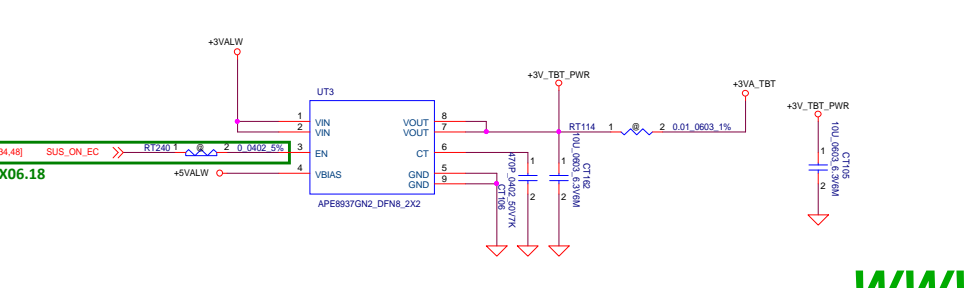
Touch Screen Load Switch & Card Reader



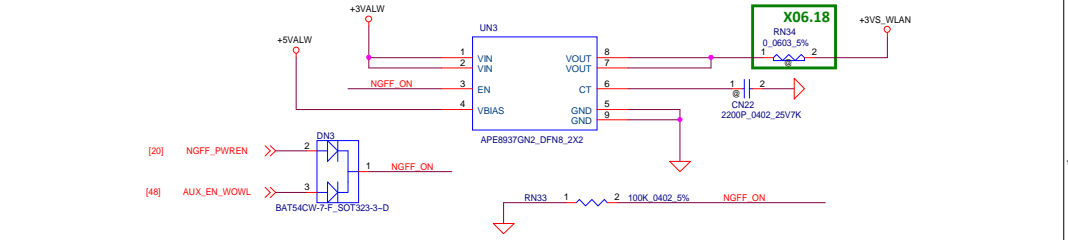
eDP & Camera Load Switch



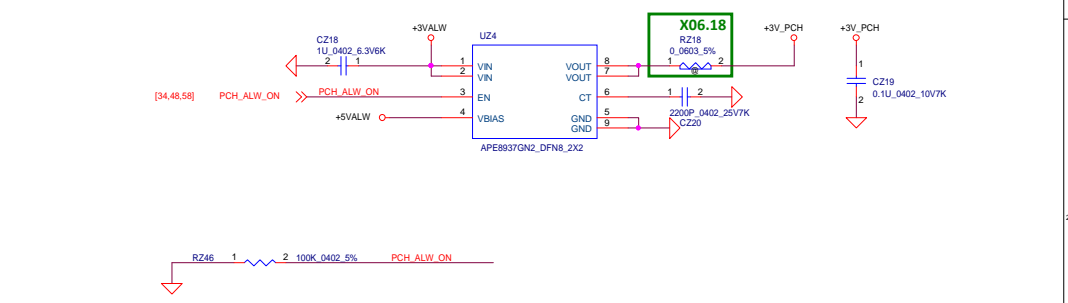
Alpine Ridge(TBT) Load Switch



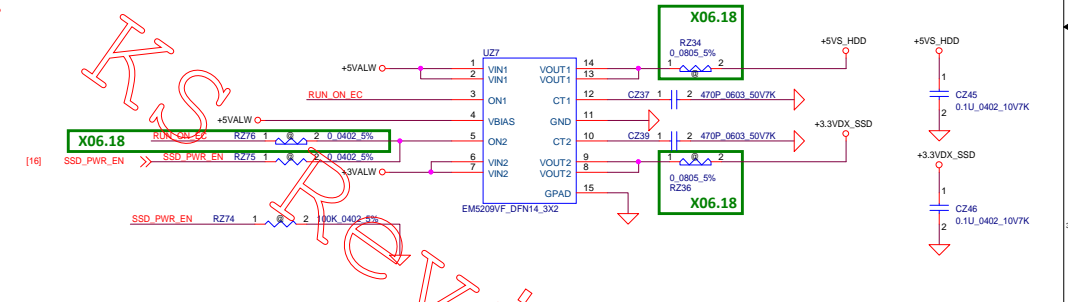
WLAN Load Switch



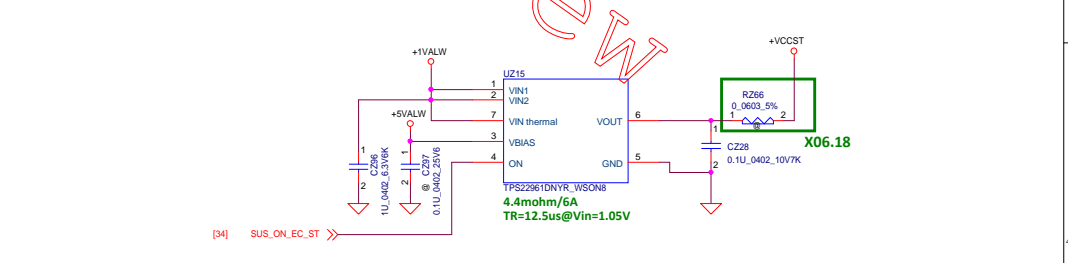
+3VALW to +3V_PCH



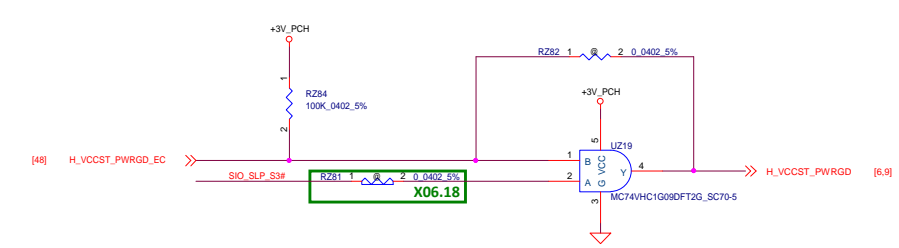
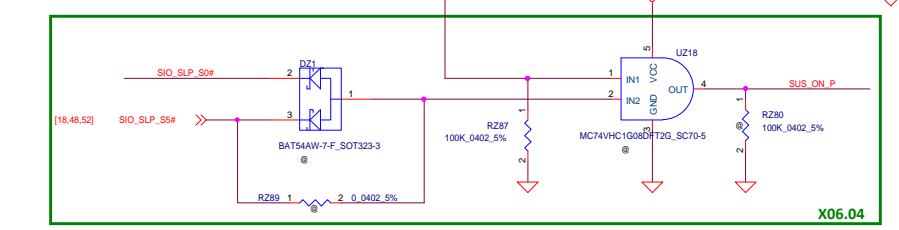
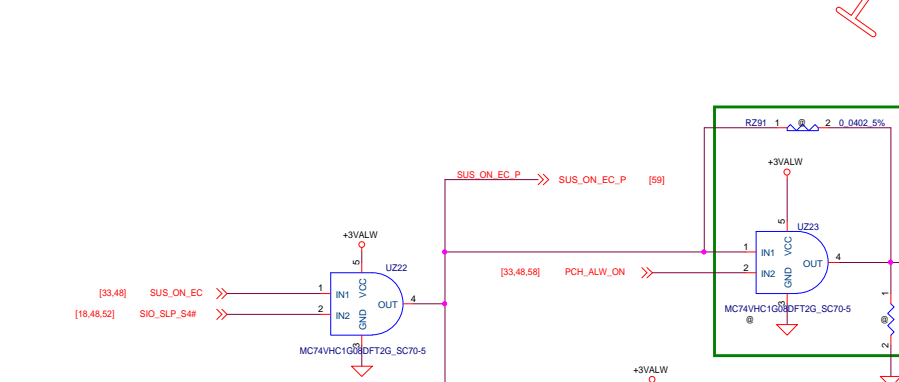
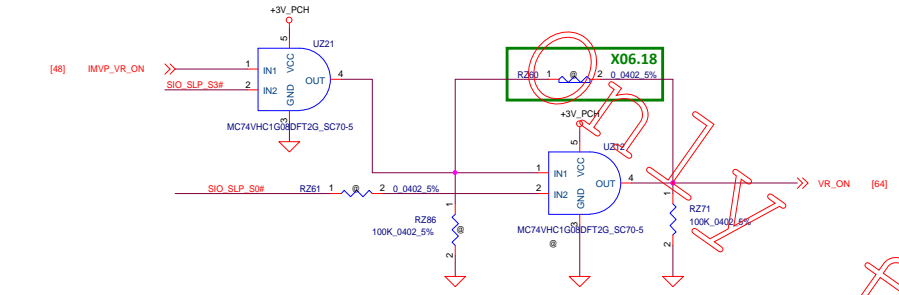
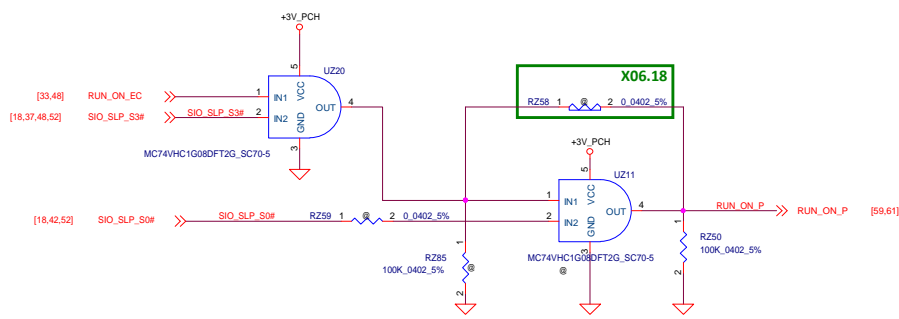
HDD, SSD Load Switch



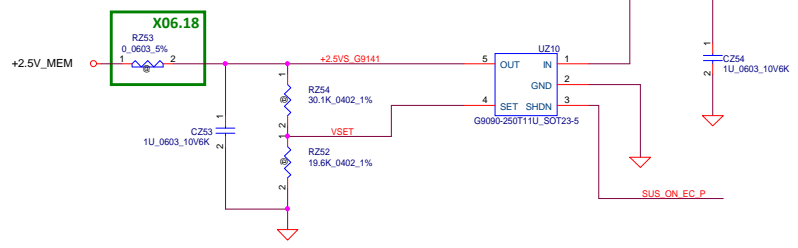
+VCCST Load Switch



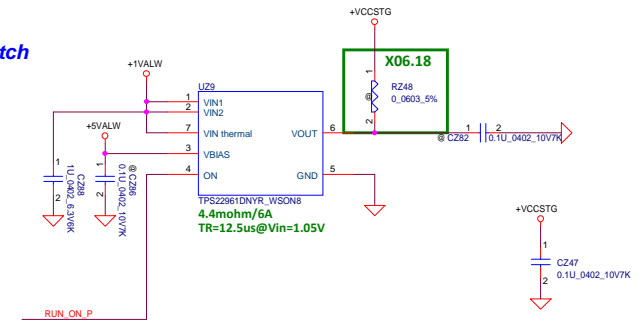
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LA-C361P				Rev 1
Date: Thursday, August 06, 2015				Sheet 33 of 71



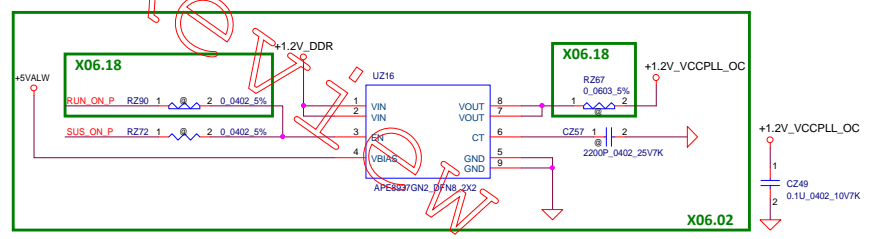
DDR4 VPP Load Switch



+VCCSTG Load Switch



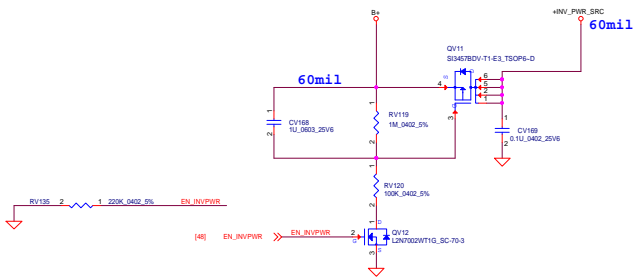
+VCCPLL_OC Load Switch



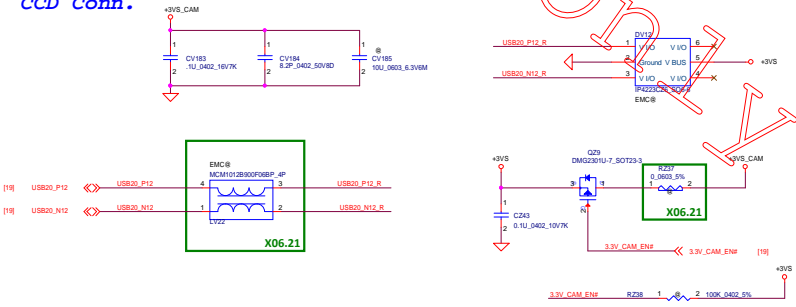
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		LA-C361P		0.1(200)	
Date:		Thursday, August 06, 2015		Sheet 34 of 71	

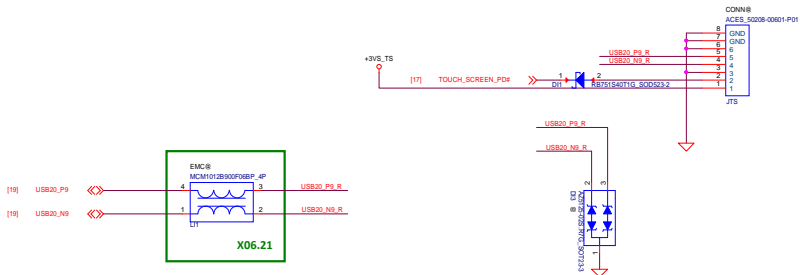
LCD backlight PWR CTRL



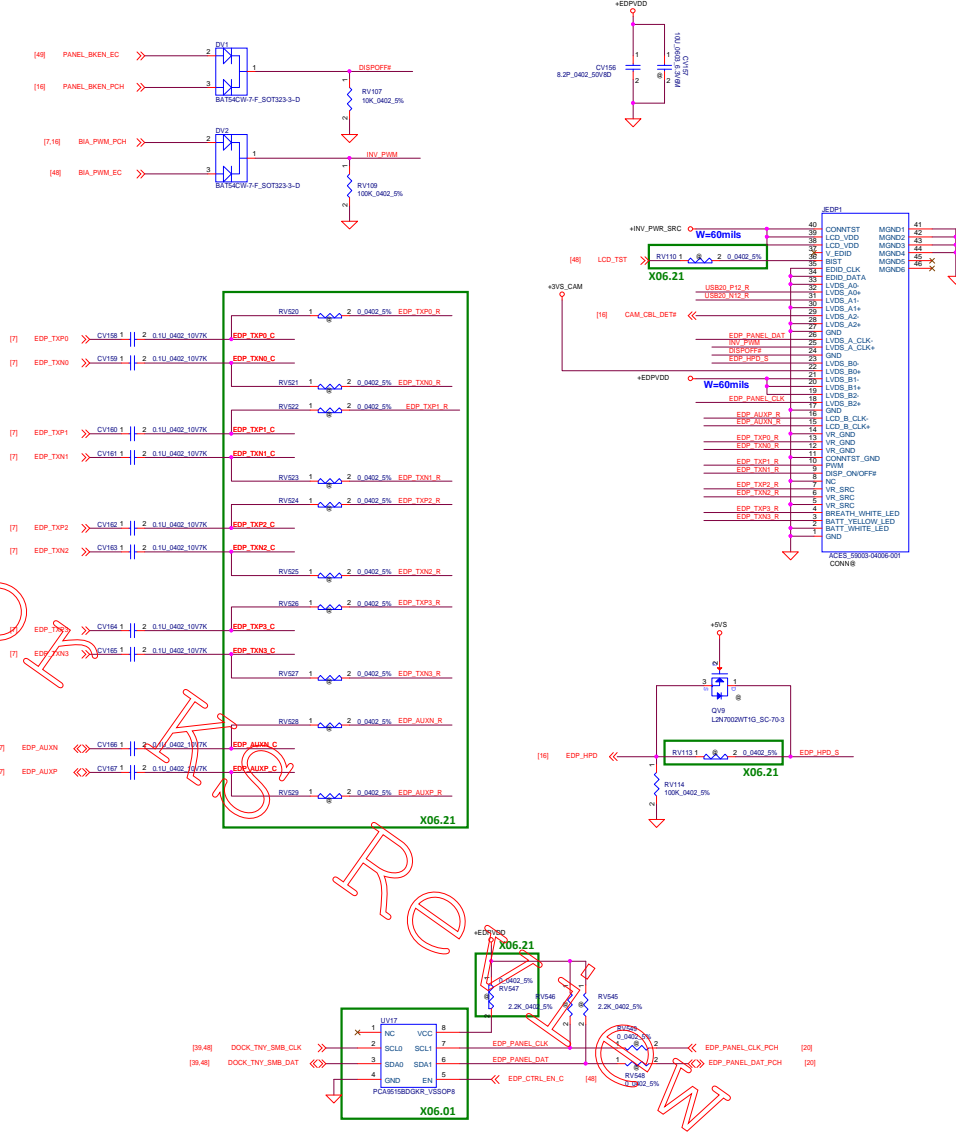
CCD Conn.

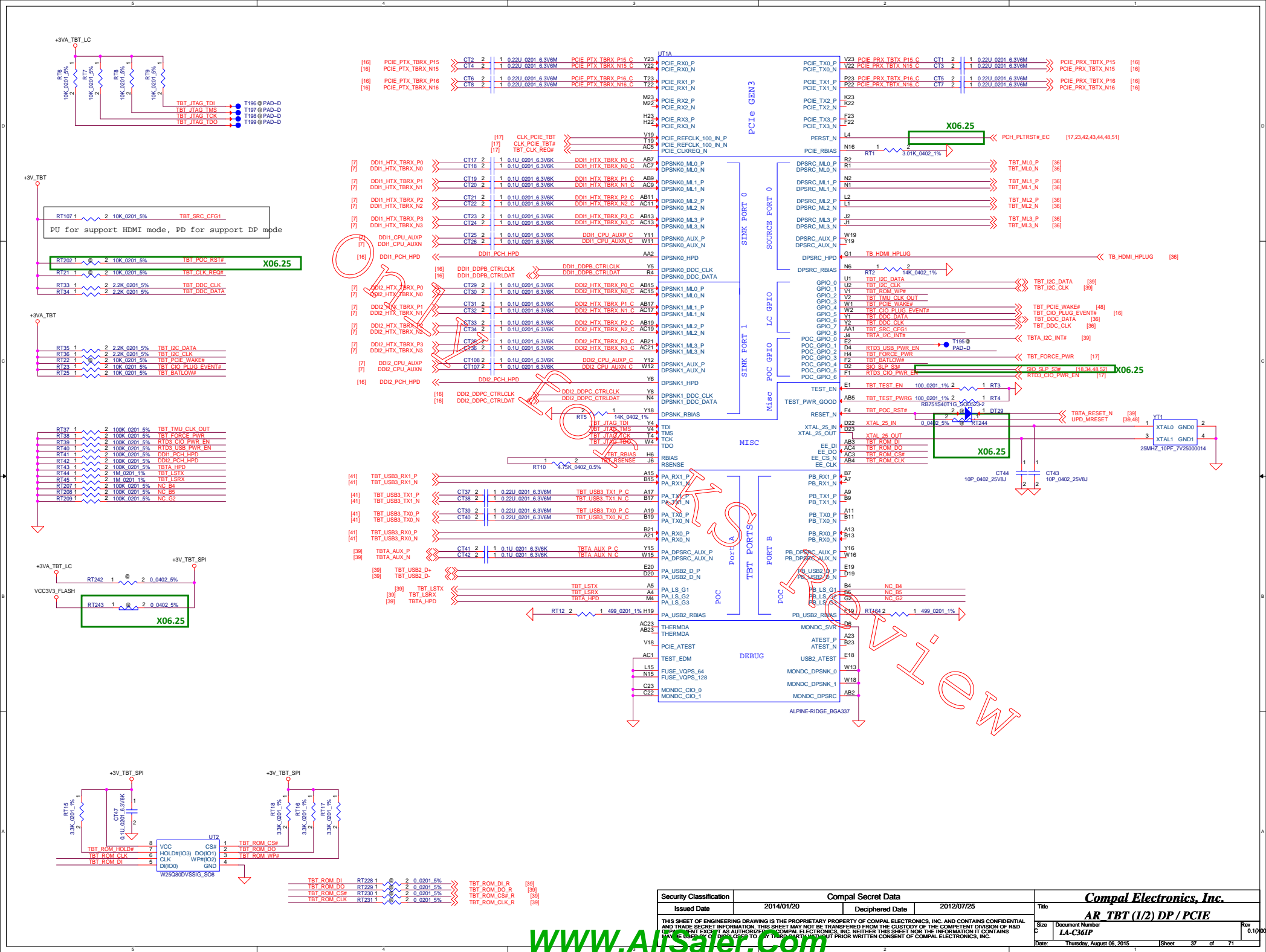


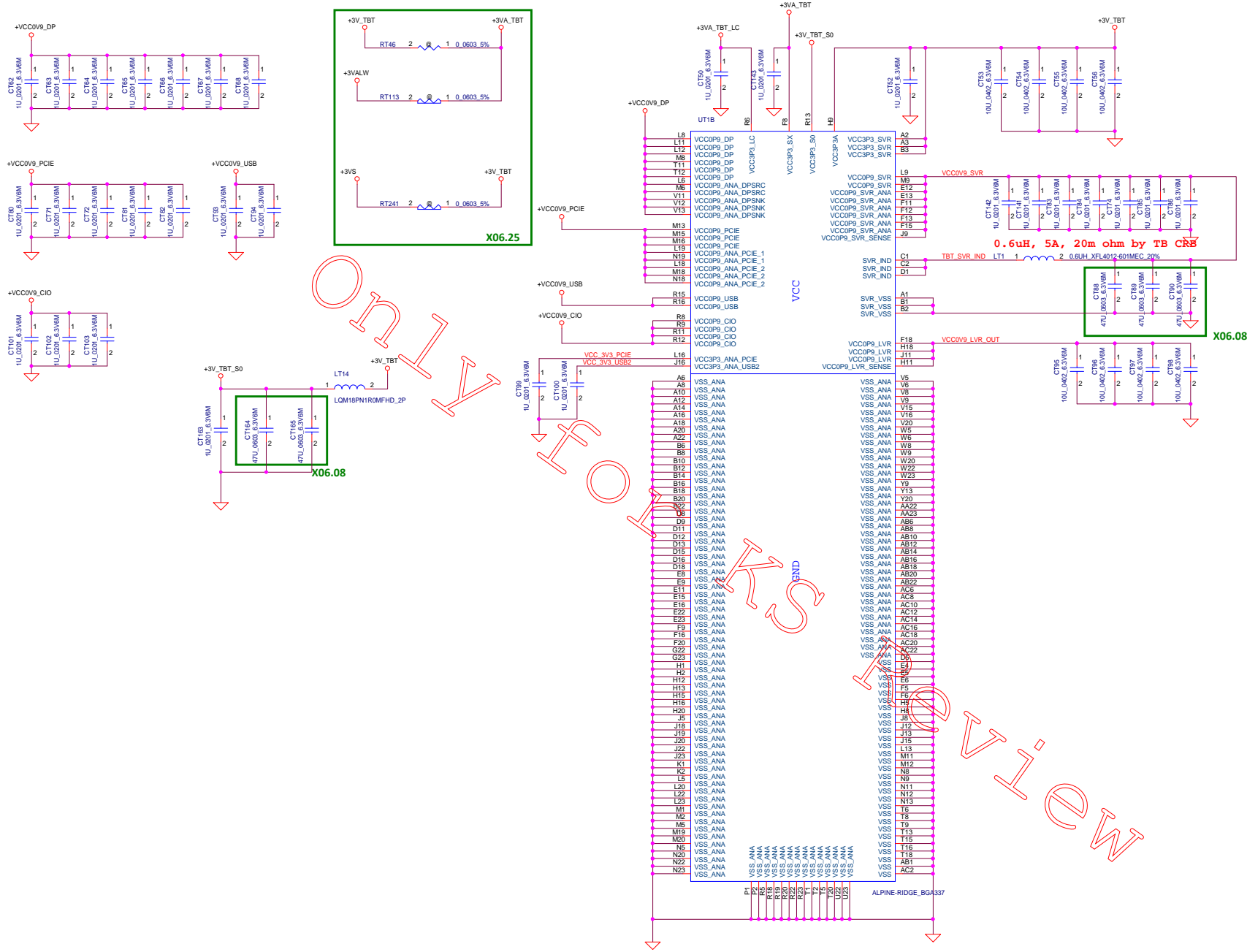
Touch Screen Conn.

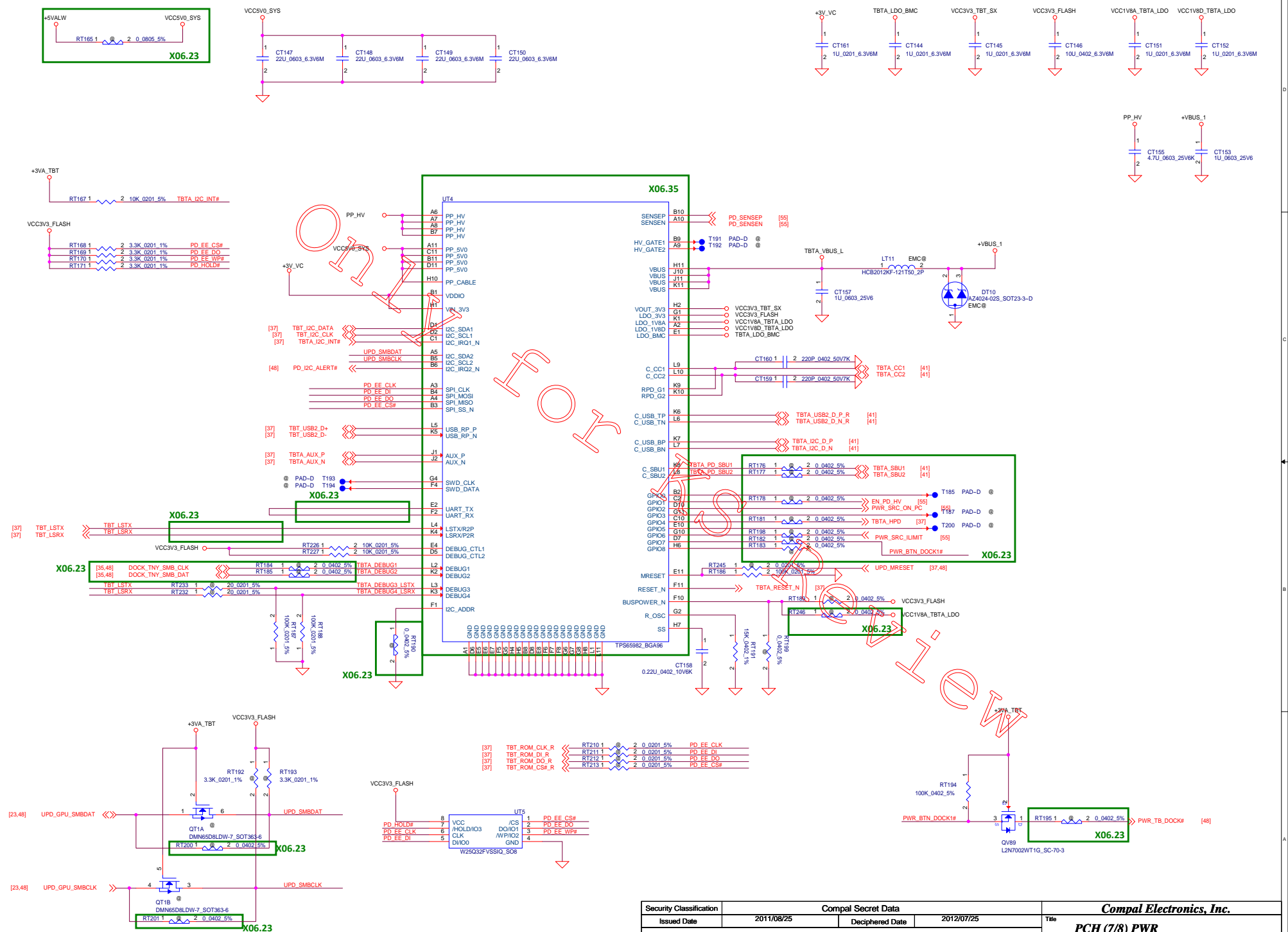


eDP & TS Conn.





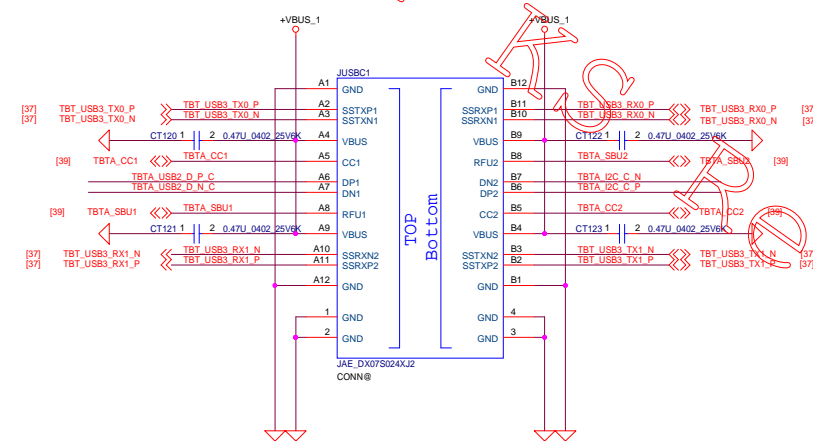
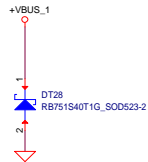
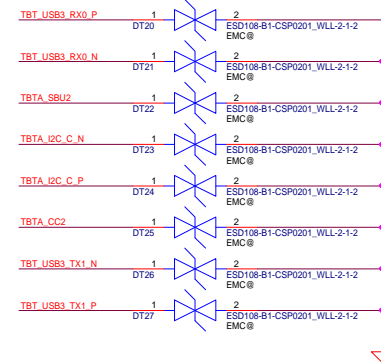
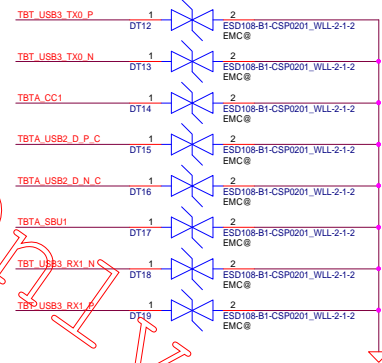
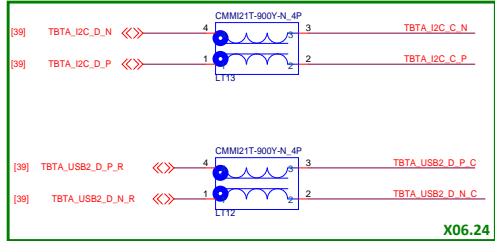




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				Sheet 40 of 71	

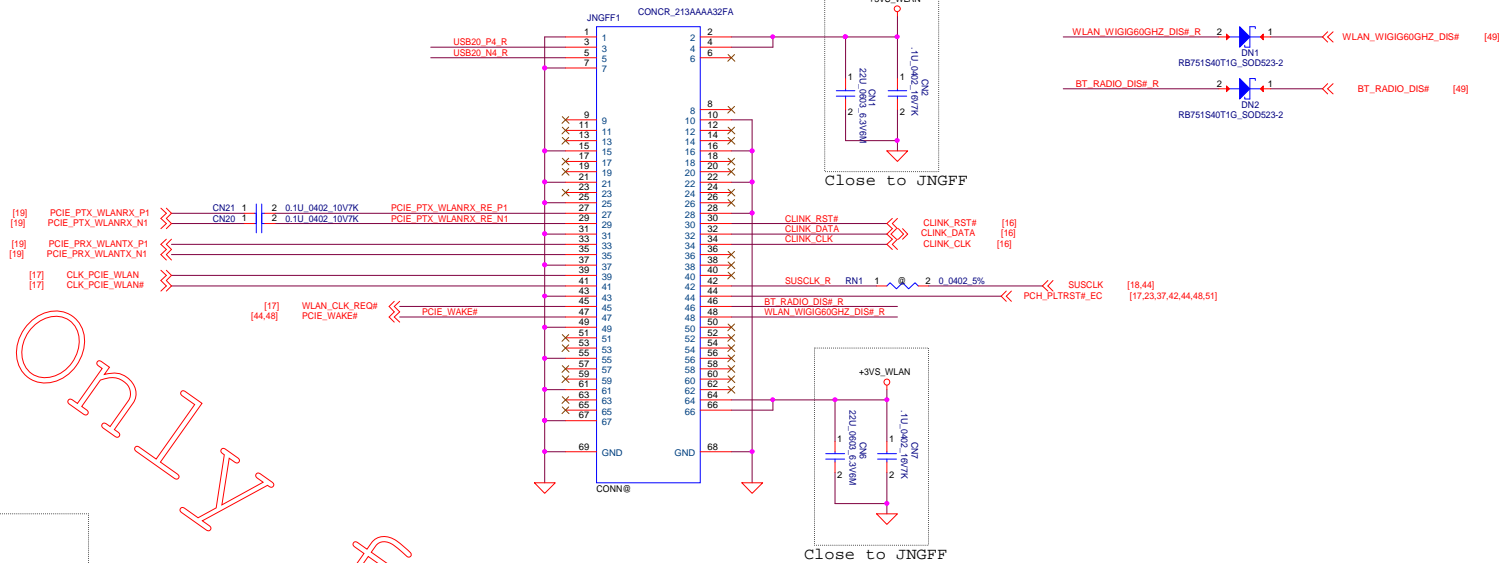
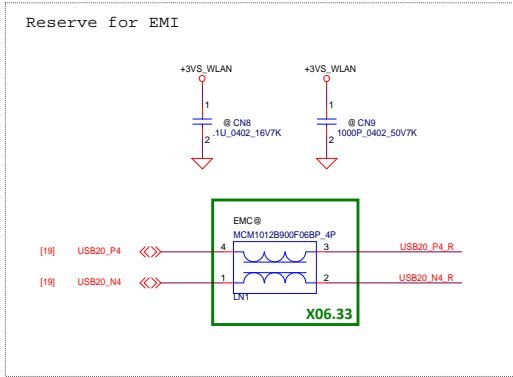


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Issued Date	2014/01/20	Deciphered Date	2012/07/25	PD USB TYPE-C	
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				Rev	0.1(00)

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M.2 Slot-A Key-A (WLAN + BT)

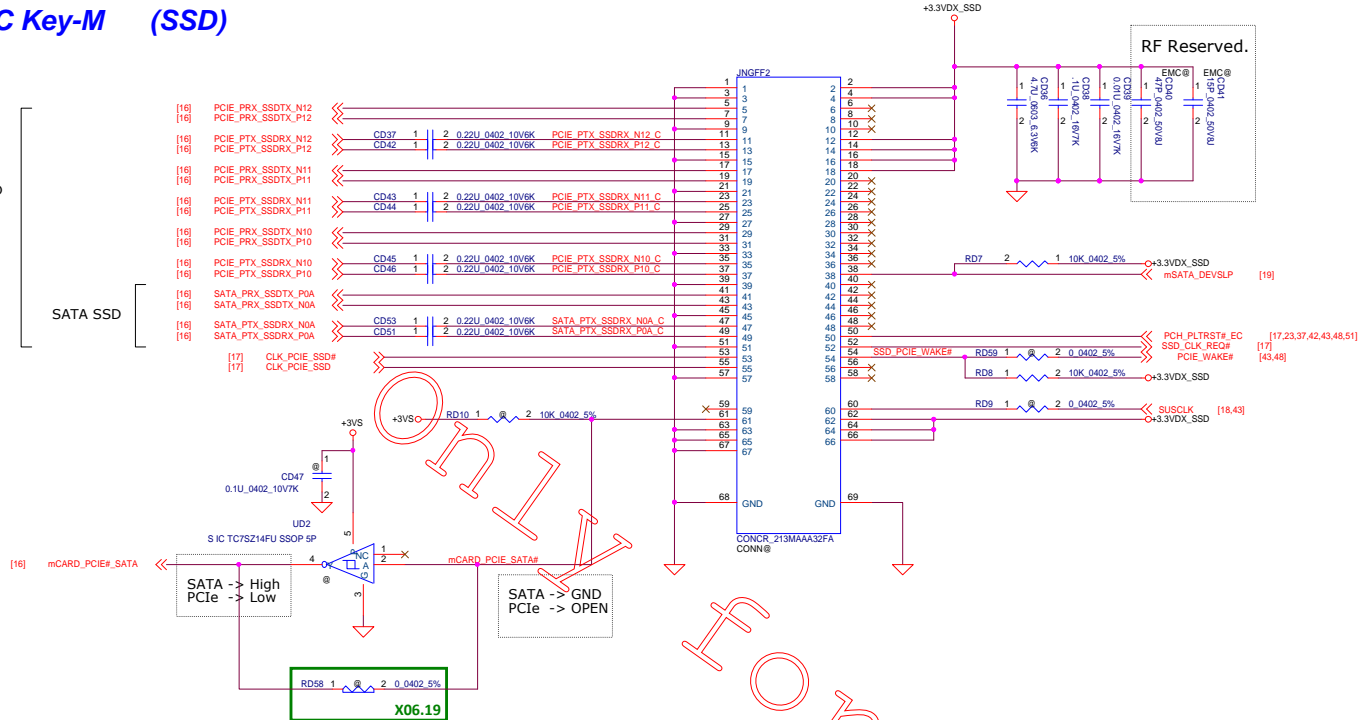
Only for KS Review



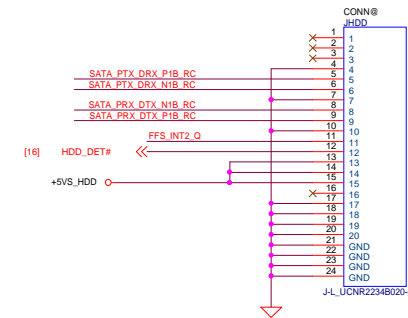
M.2 Slot-C Key-M (SSD)



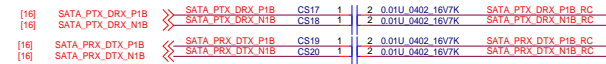
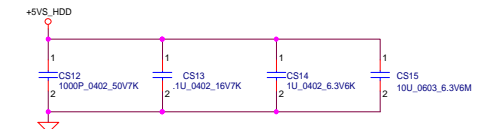
SATA SSD



HDD CONN

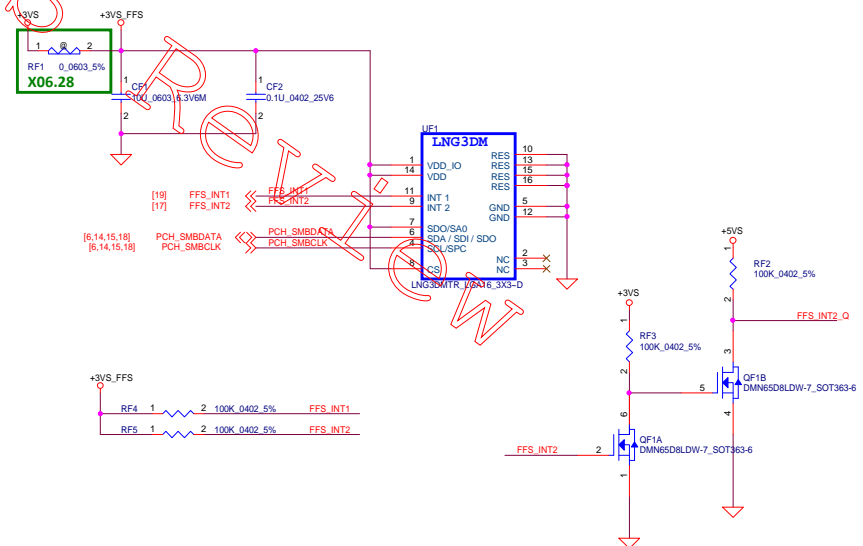


Place near HDD CONN (JHDD1)



BYPASS Circuit

Free Fall Sensor

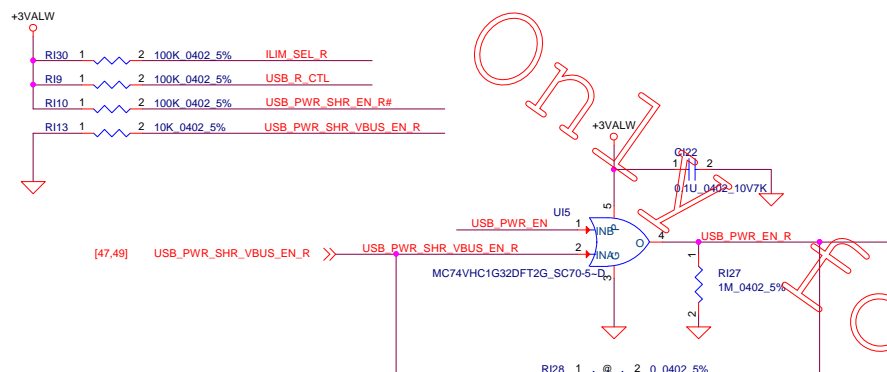


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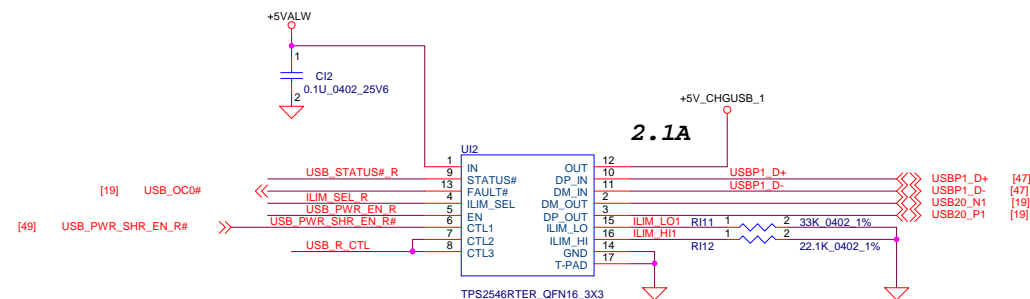
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

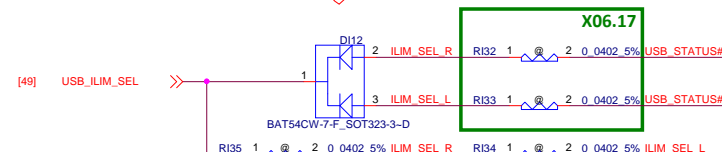
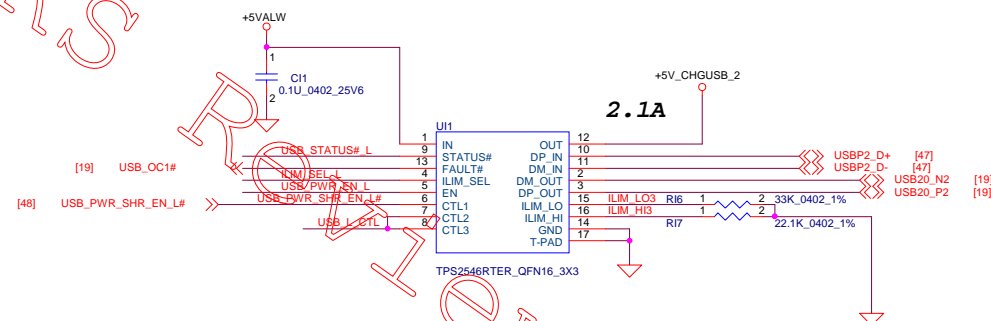
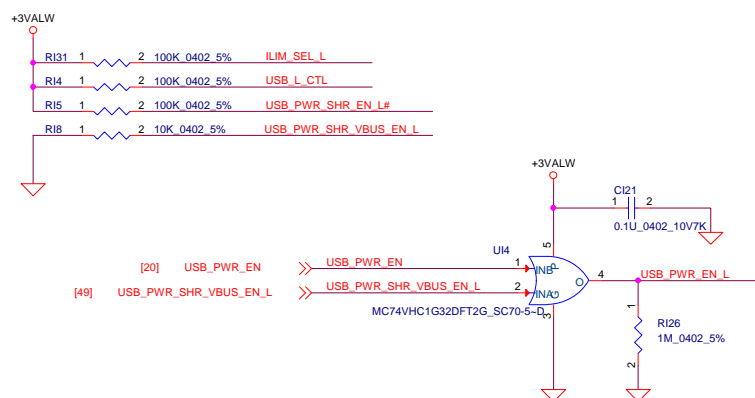
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)



USB3.0 / USB2.0 Port1 (Right Side)

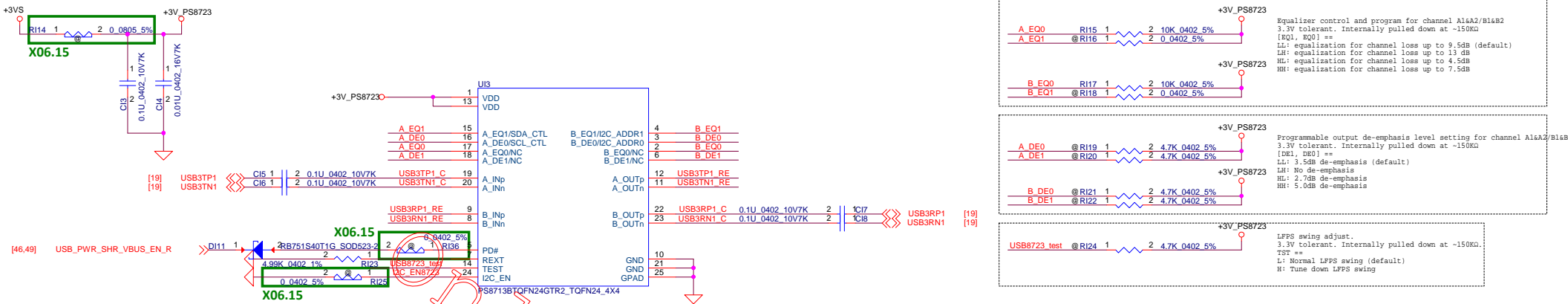


USB3.0 / USB2.0 Port2 (Left Side)

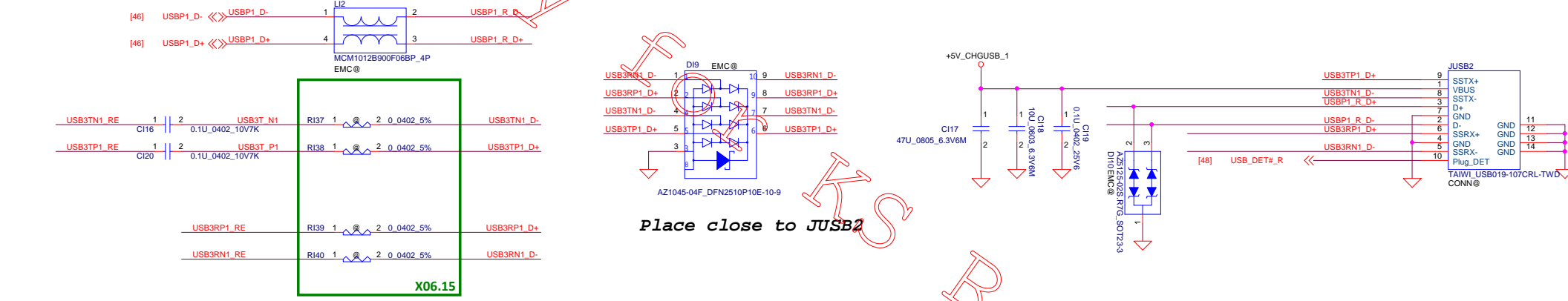


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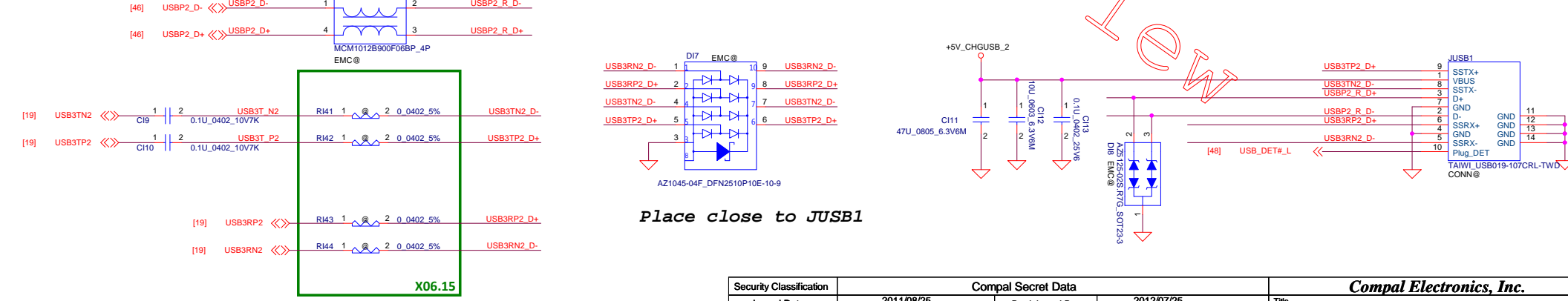
USB3.0 Re-driver



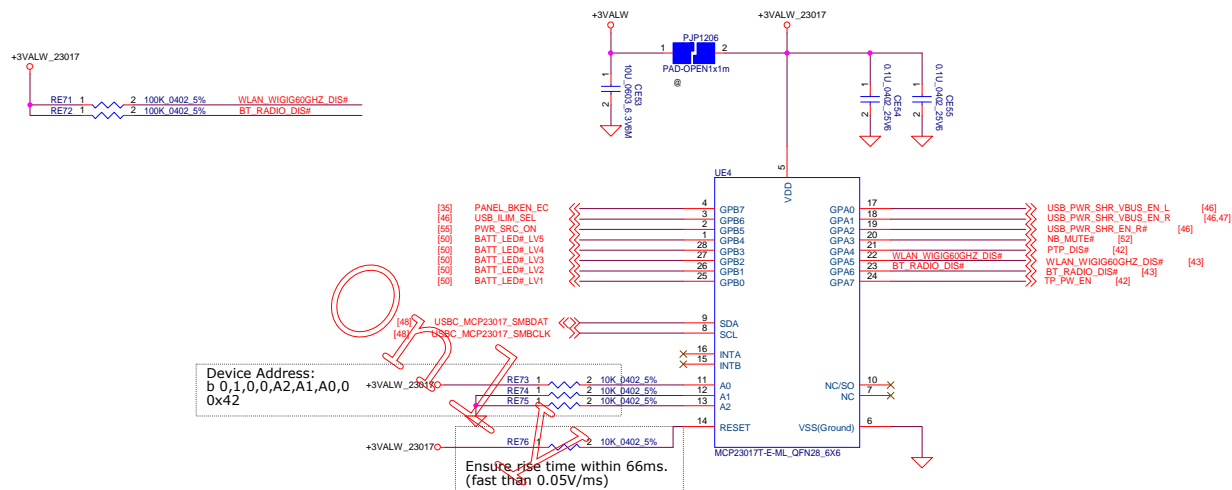
USB3.0 / USB2.0 Port1 (Right Side)



USB3.0 / USB2.0 Port2 (Left Side)

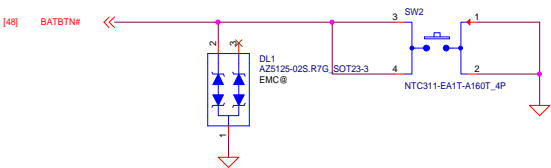


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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	USB conn.
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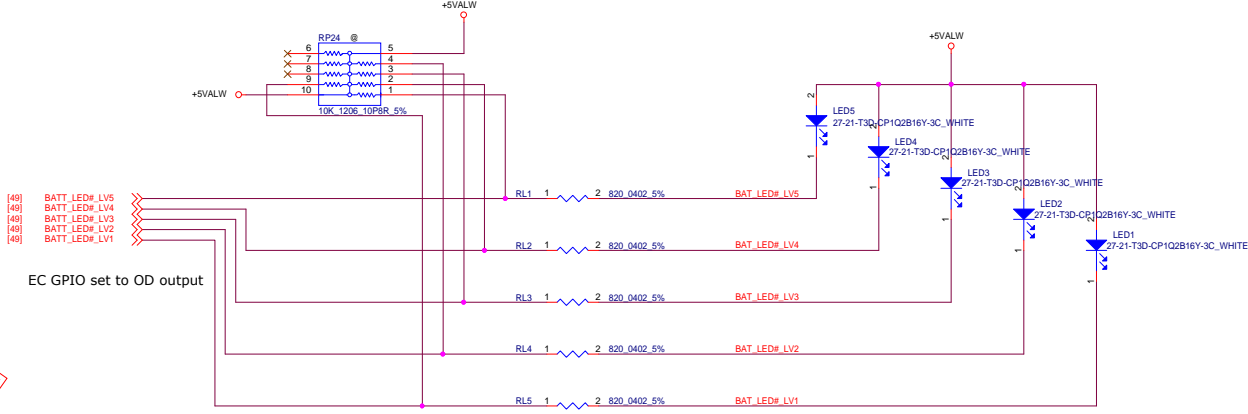


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/08/25	Deciphered Date	2012/07/21	Title
					AMP TPA3113/SPK conn.
Size	C	Document Number	LA-C361P		Rev
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BATT LED Power Button

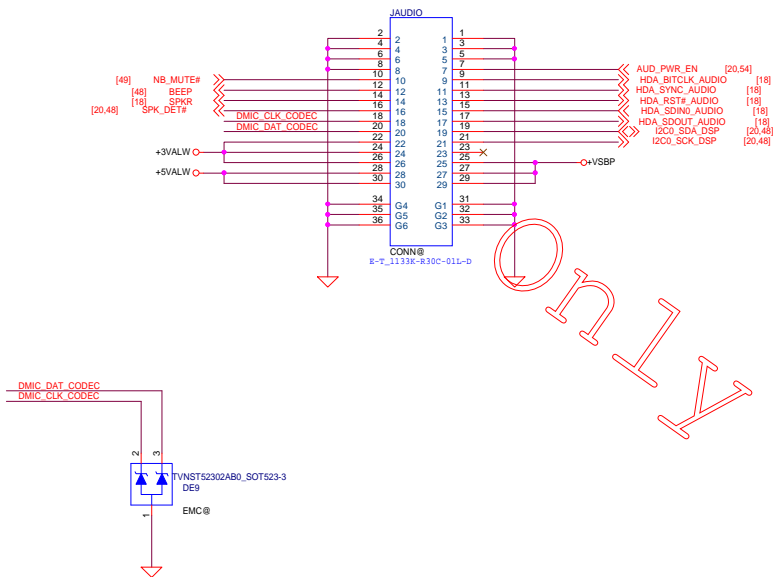


Battery Gauge LED

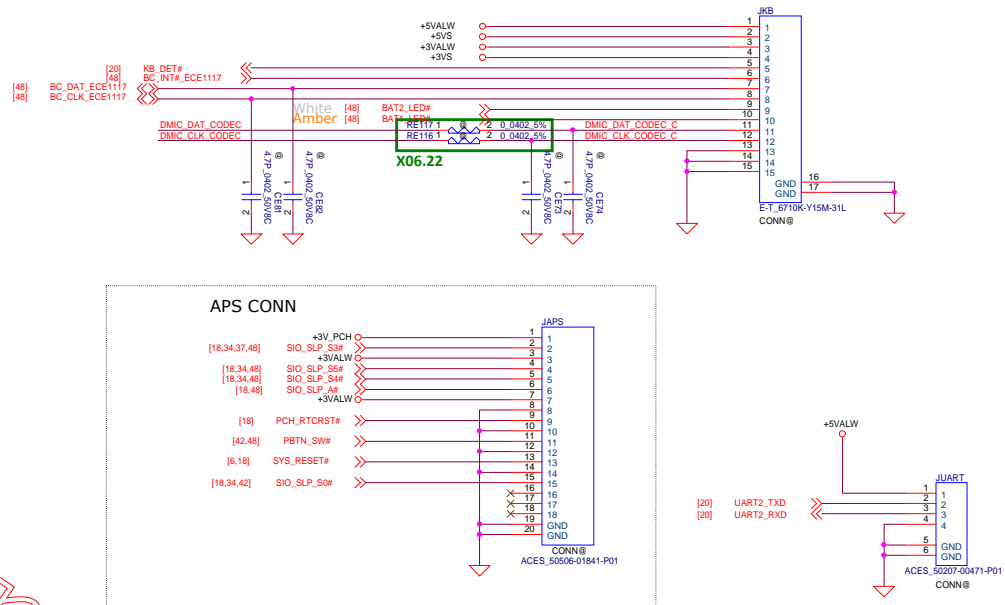


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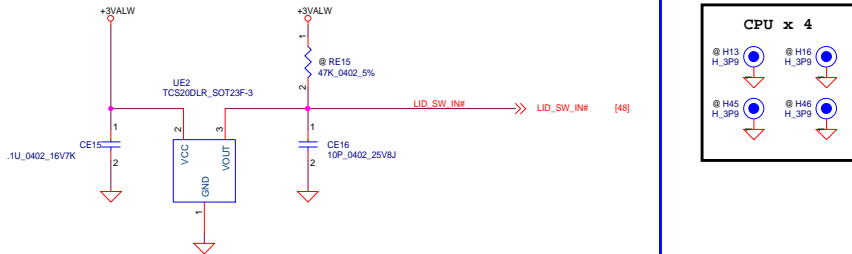
AUDIO Board Conn.



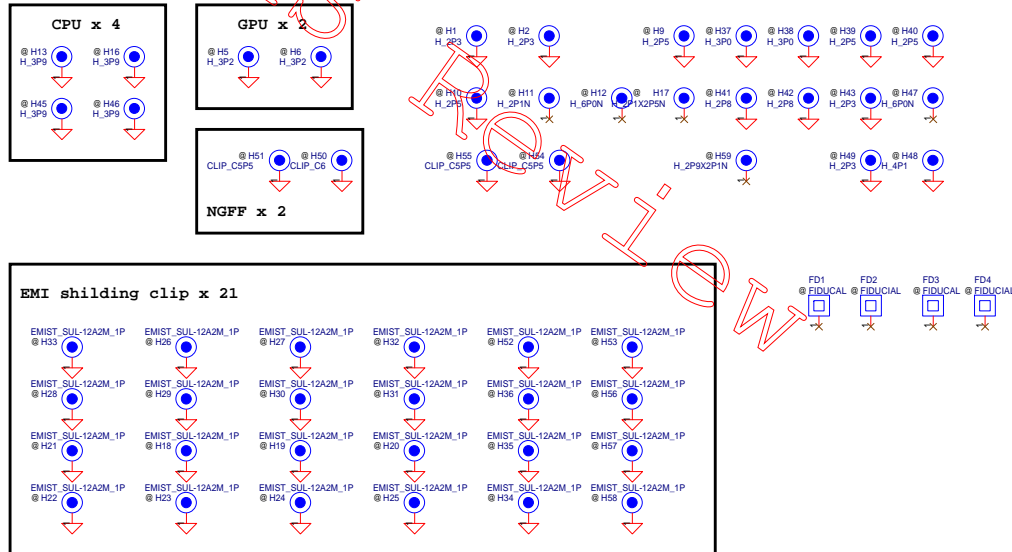
Keyboard Controller board + DMIC



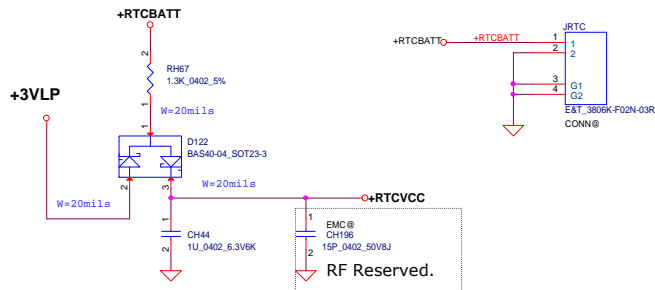
Lid Switch



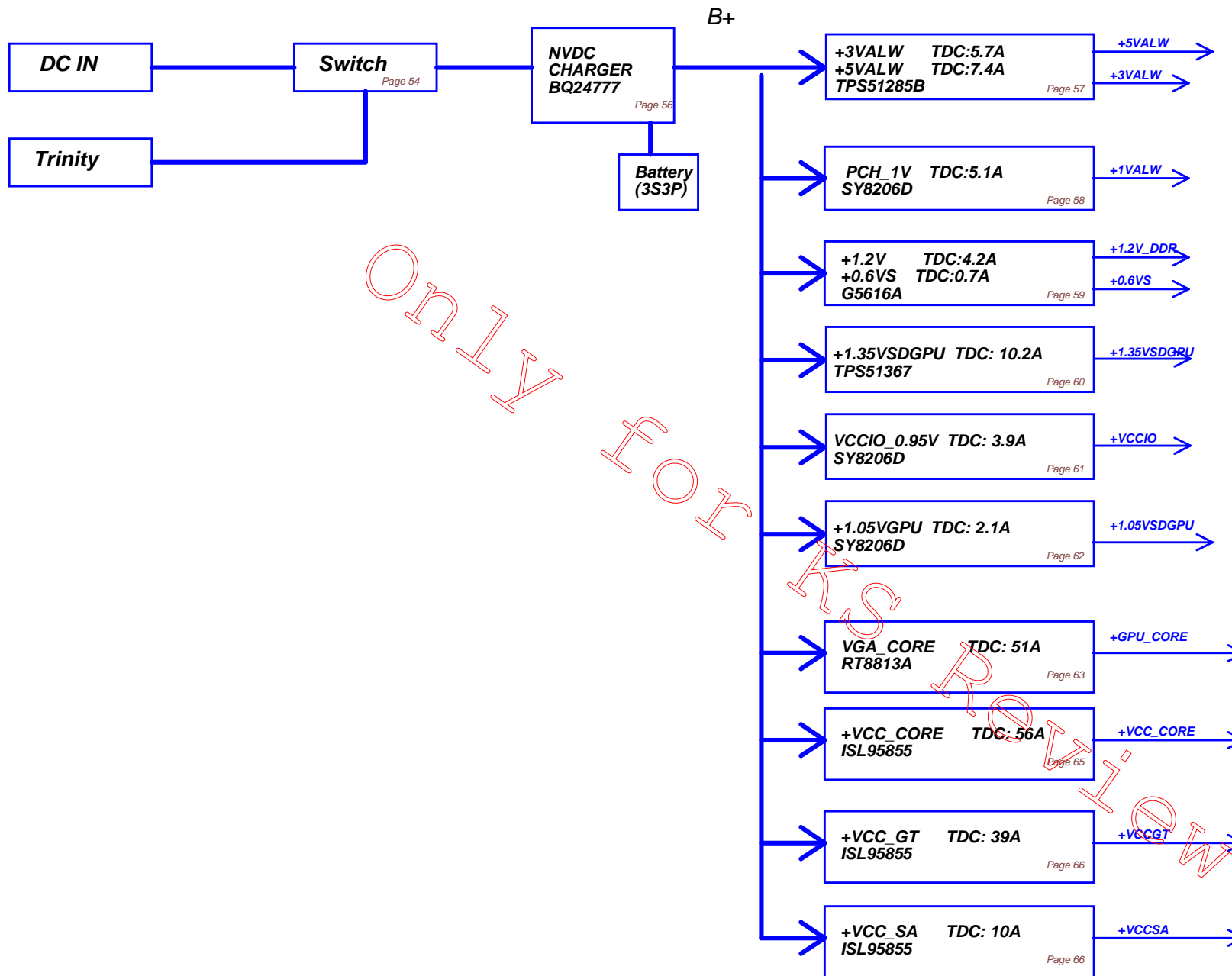
Screw Hole



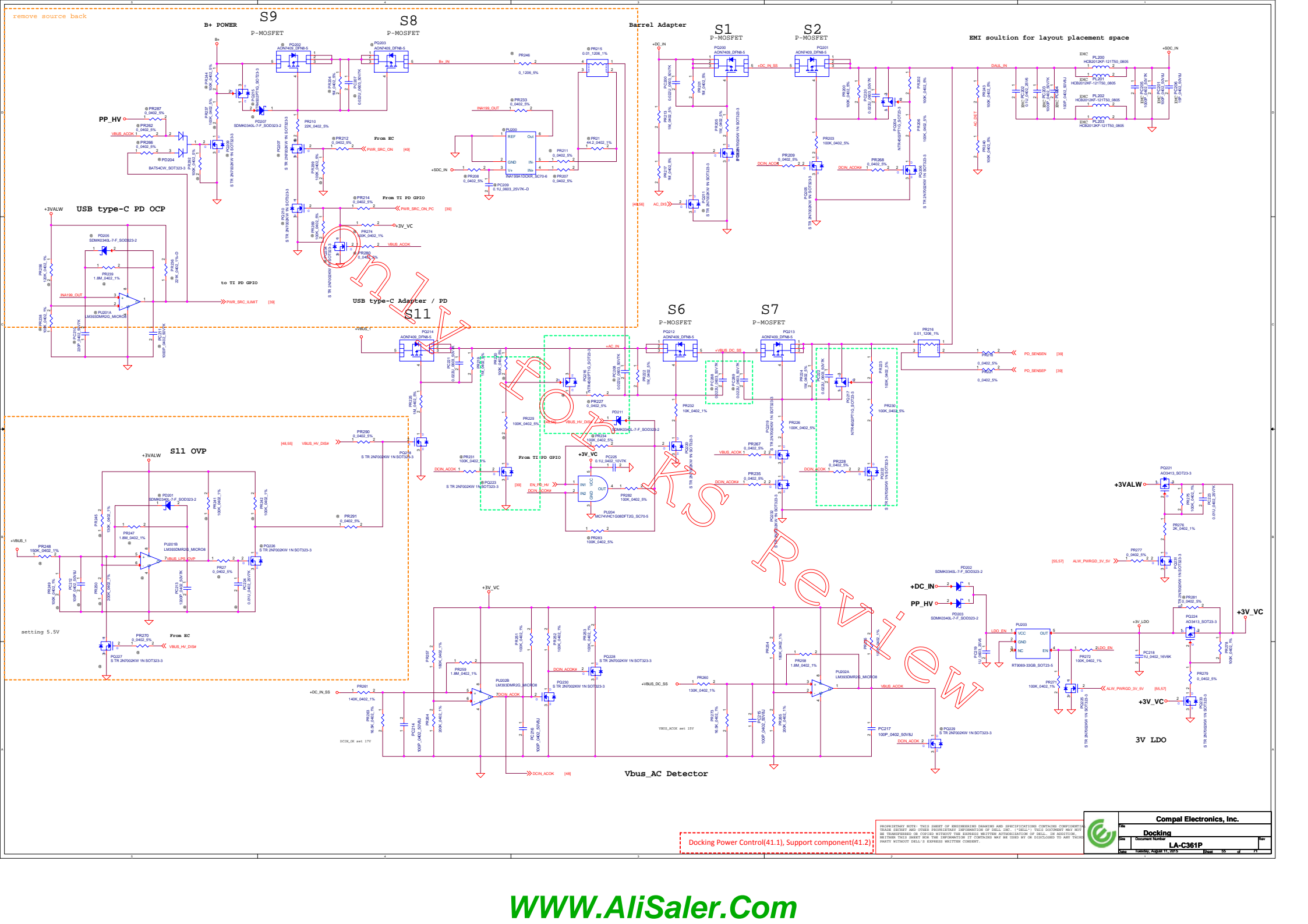
RTC Battery With Charge Function

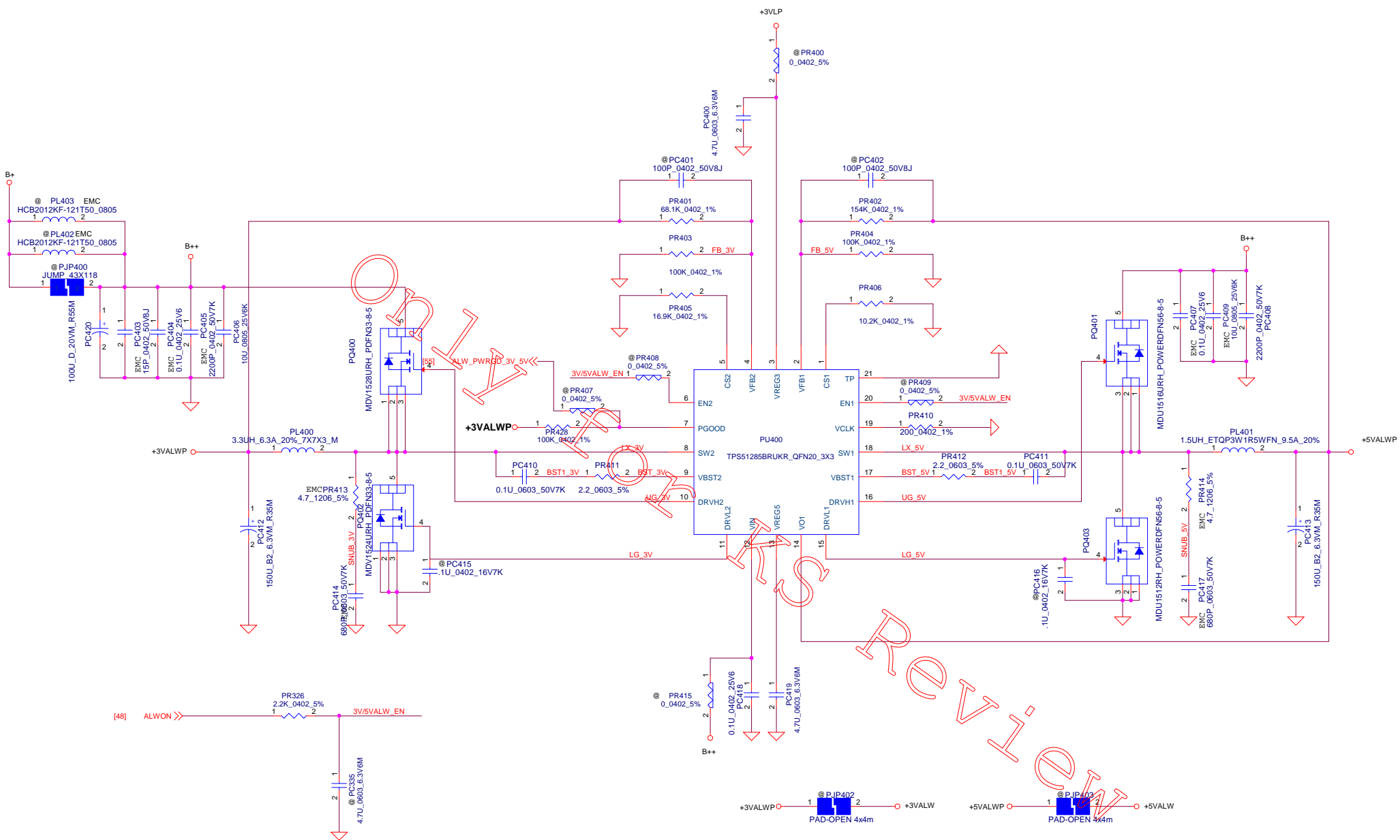


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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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2011/08/25		2012/07/25		Power Sequence diagram	
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					0.1(P00)
		Date:		Tuesday, August 11, 2015	Sheet 53 of 71





3.3VALWP
TDC 5.7A
Peak Current 8.1A
OCP current 9.7A

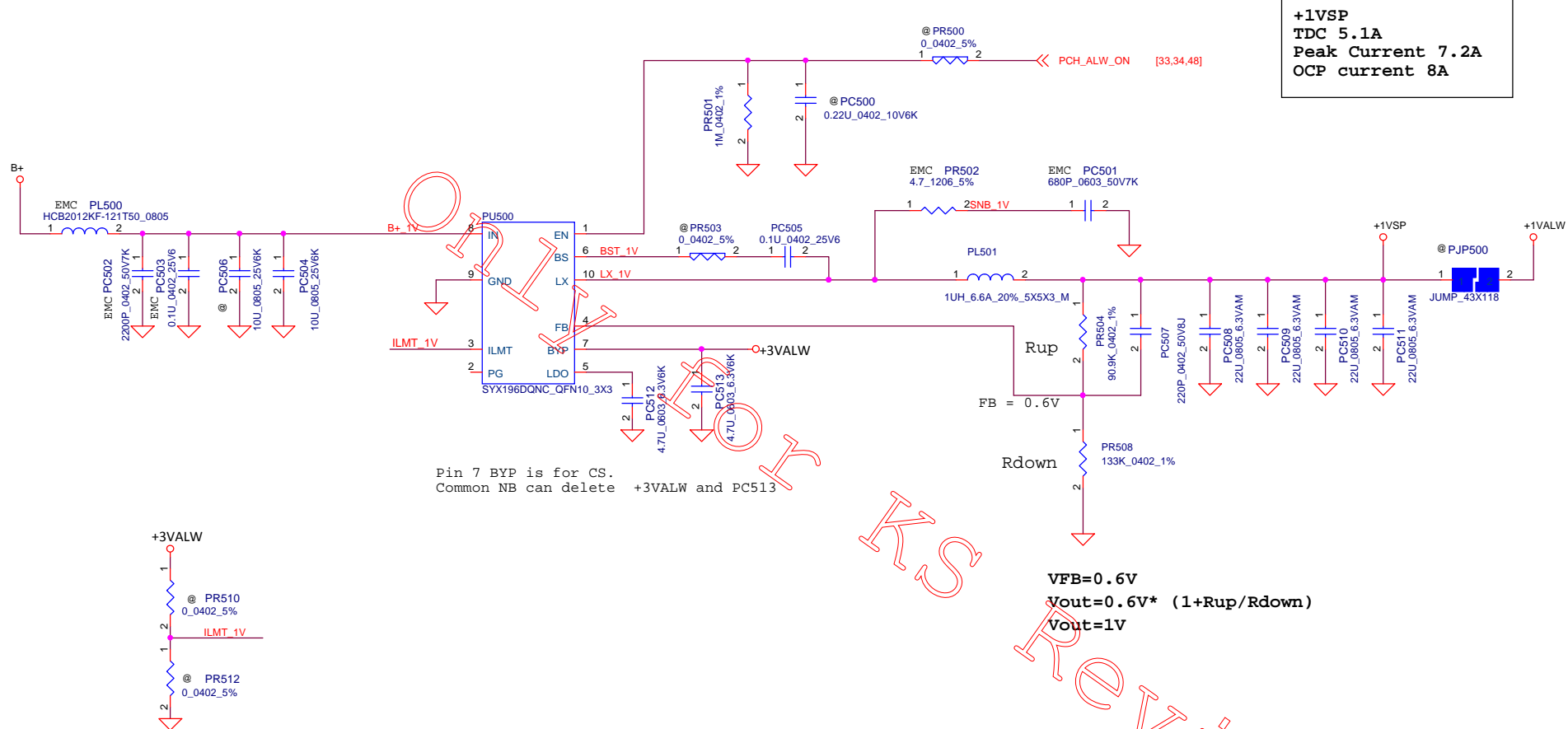
5VALWP
TDC 7.4A
Peak Current 10.5A
OCP current 12.6A

3V/5V controller(35.1), Support component(35.2)

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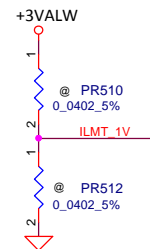
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Compal Electronics, Inc.			
Title			
PWR-3VALWP/5VALWP			
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+1VSP
TDC 5.1A
Peak Current 7.2A
OCP current 8A

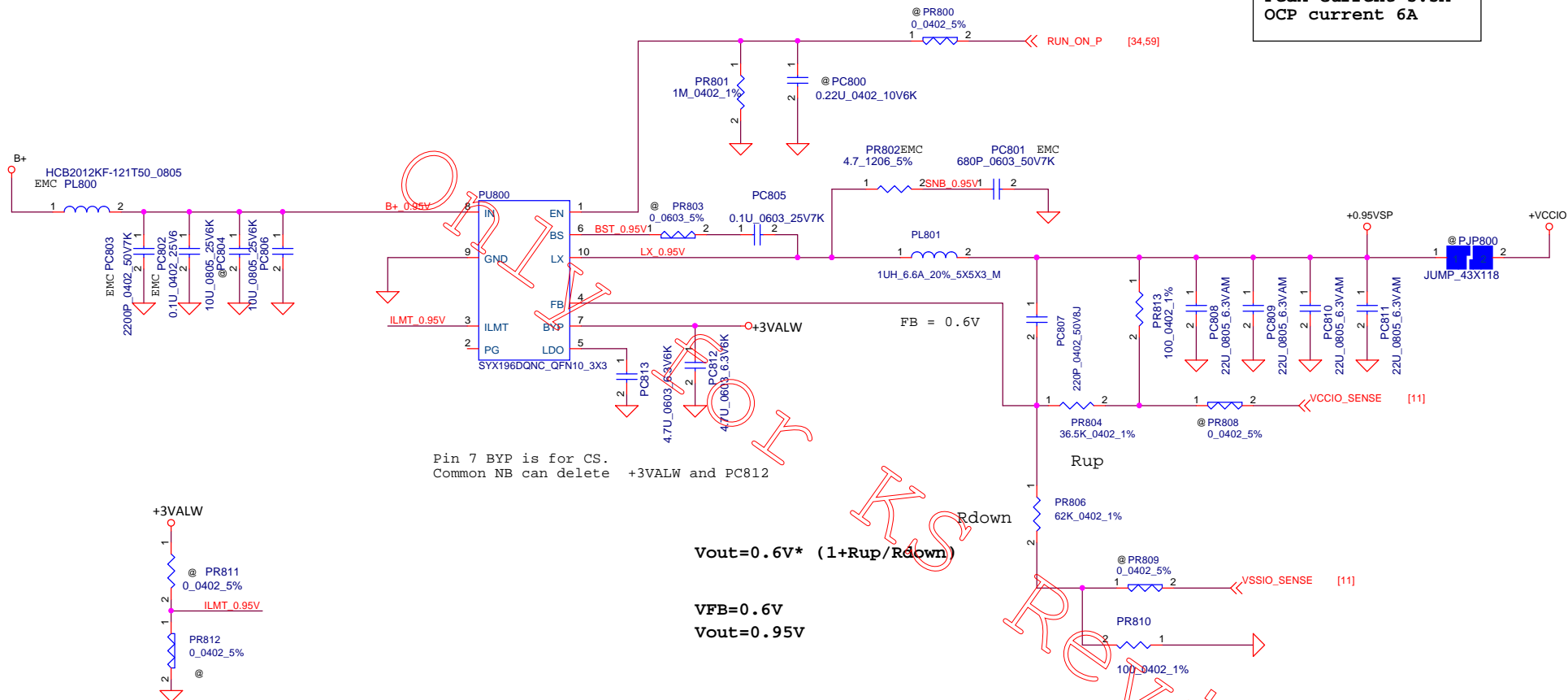
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC513



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

PWR.Plane.Regulator(35.25), Support component(35.26)

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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P40-PWR +IVA
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The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

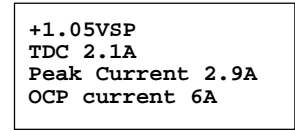
1.05V controller(35.5), Support component(35.6)

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC812

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

VFB=0.6V
Vout=0.95V

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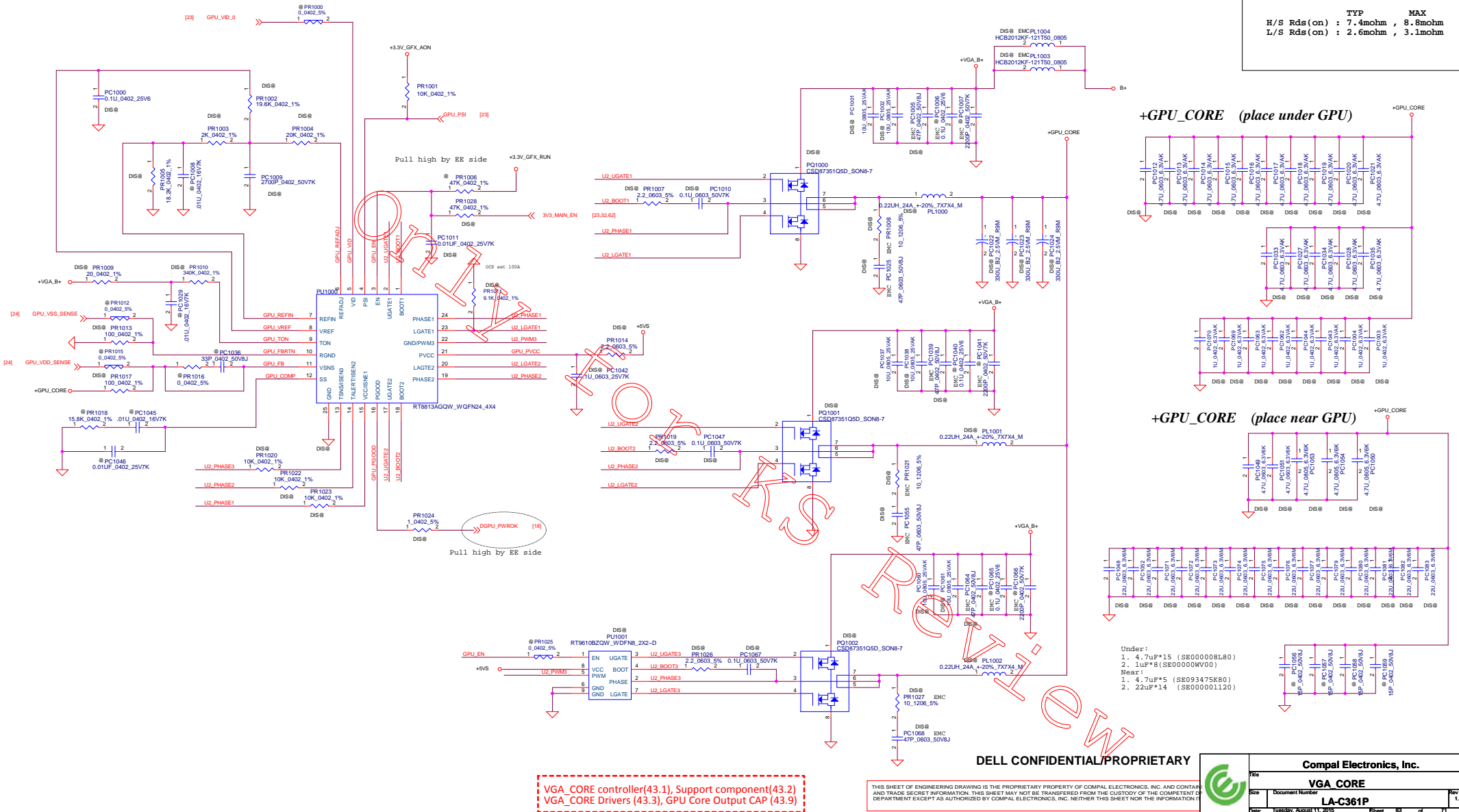
VFB=0.6V
 $V_{out}=0.6V \cdot (1+R_{up}/R_{down})$
~~Vout=1.05V~~

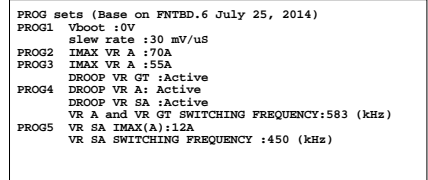
GPU other power_Regulatorr(43.7), Support component(43.8)

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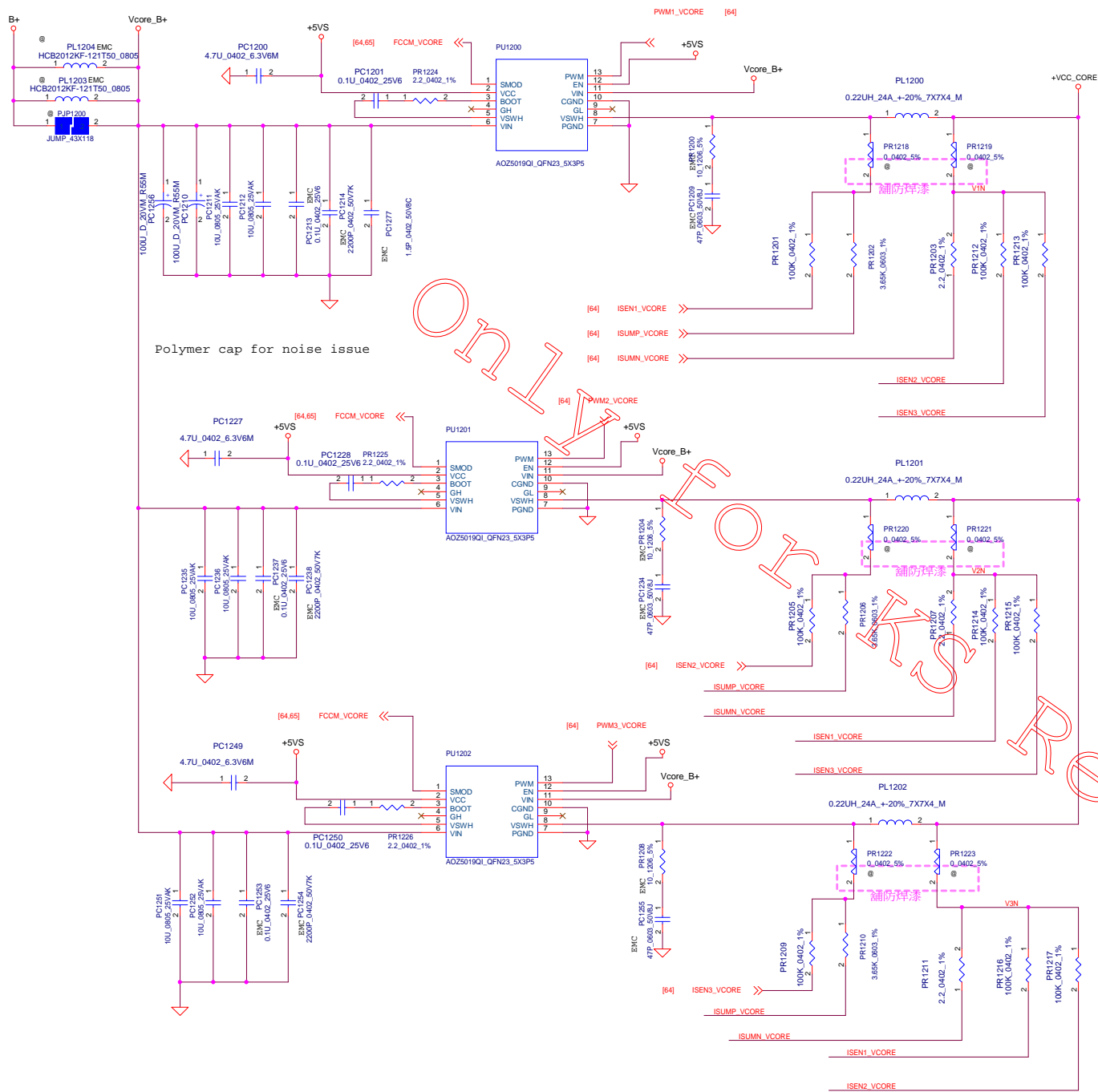
GPU_CORE (0.95V)
TDC 51A
Peak Current 87A
OCP current 100A
DCR 0.97mohm +/- 5%

	TYP	MAX
H/S Rds(on) :	7.4mohm	8.8mohm
L/S Rds(on) :	2.6mohm	3.1mohm





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Polymer cap for noise issue

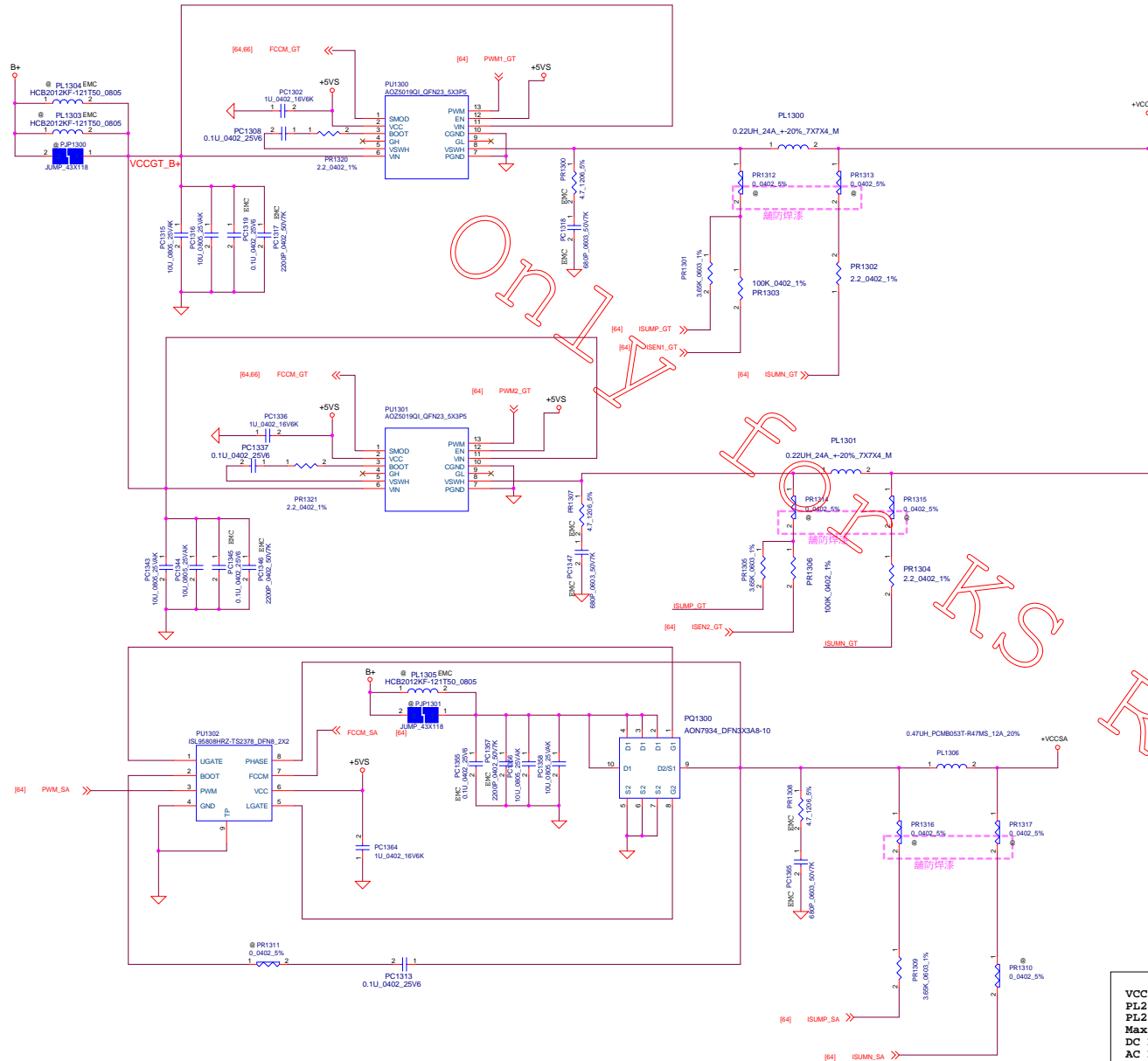
VCC_core (Base on PDDG rev 0.7)
 PL2 TDC_default):TB
 PL2 TDC_max (40Sec):56A
 Peak Current 68A
 DC Load line ~1.8mV/A
 AC Load line ~1.8mV/A
 OCP Current 83.2A
 DCR 0.97mohm +/-5%

CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3),
 CPU_Vcore output CAP(36.4), Acoustic Noise B+ Bulk CAP(37.2)

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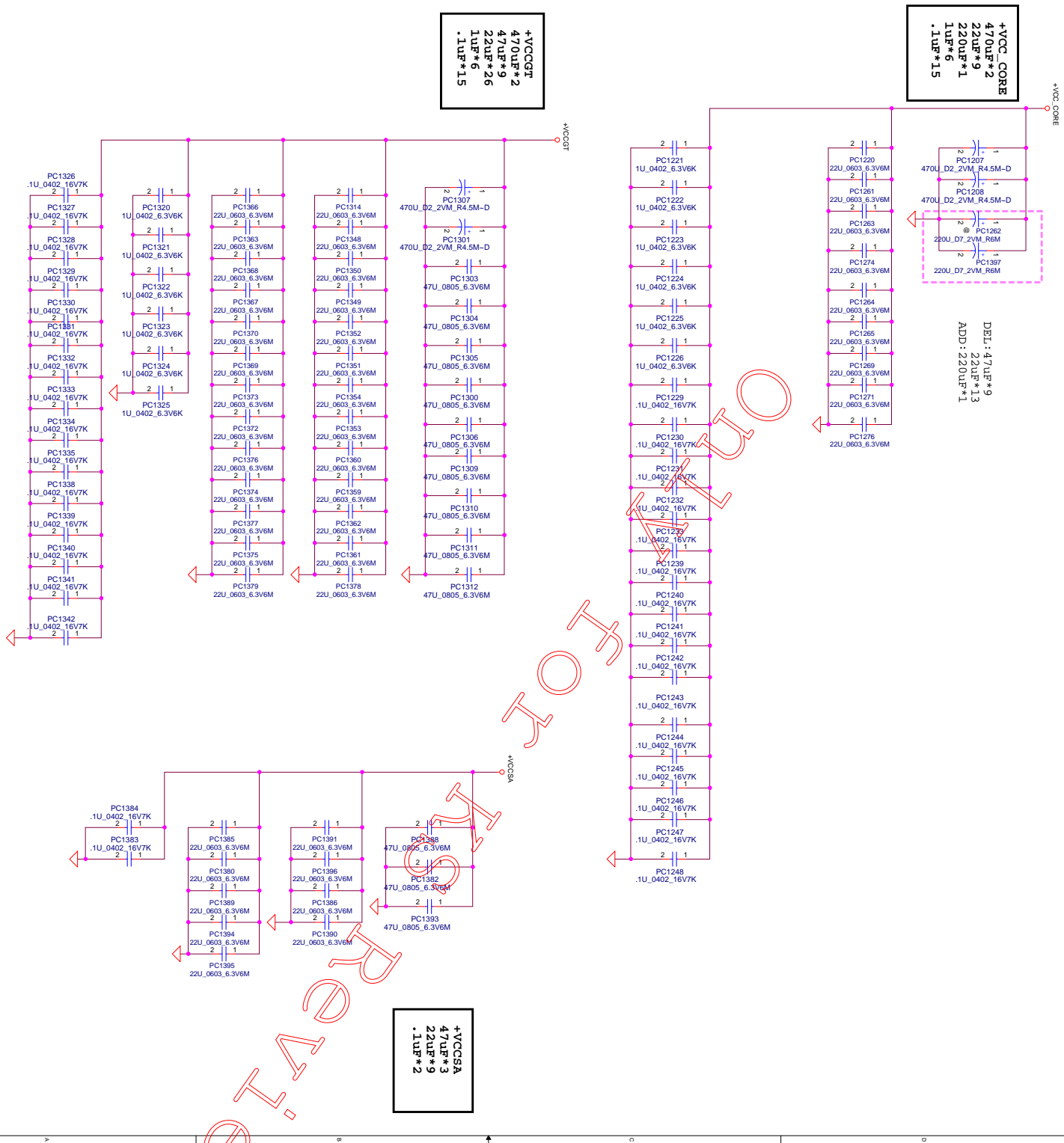
VCCGT (Base on PDDG rev 0.7)
 PL2 TDC_default):TB
 PL2 TDC_max (40Sec):39A
 Max Current 55A
 DC Load line -2.65mV/A
 AC Load line -2.65mV/A
 OCP Current 66.7A
 DCR 0.97mohm +/-5%



VCCSA (Base on PDDG rev 0.7)
 PL2 TDC_default):TBD
 PL2 TDC_max (40Sec):10A
 Max Current 11A
 DC Load line -9.1mV/A
 AC Load line -9.1mV/A
 OCP Current 20A
 DCR 7.4mohm/8.5mohm +/-5%

CPU_Vcore controller(36.1), Drivers(36.2), Support component(36.3),
 GFX output CAP(36.5)

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1	6	XDP	2014/12/12	EE	Change Pull high power for leakage issue	Change RH494,RH495,RH496 from +VCCST to +VCCSTG, de-POP RH97,RH98,RH100, POP RH494,RH495.	X01
2	18	GPIO	2014/12/12	EE	Change Pull high power for double pull high the same power rail	Change RH571 power rail from +3VS to +3V_PCH, de-pop RH571, delete RH532.	X01
3	18	SPI	2014/12/12	EE	Change SPI ROM for ME register setting	Change UH8 from W25Q128FVSIQ_S08 to W25Q128FVSIQ_S08	X01
4	18	S0iX	2014/12/12	EE	Change by pass circuit design for CS mode function	Change RZ58 connection from UZ11.2 to UZ11.4, Change RZ60 connection from UZ12.2 to UZ12.4	X01
5	18	+1V_MPHY	2014/12/12	EE	Delete +1V_MPHY load switch & discharge circuit for useless.	Delete RH514,RH559,RH144,QH9,UH13,CH193,CH194,CH195. Delete net MPHP_PWR_EN, move RZ70 to page 21	X01
6	18	PD	2014/12/22	EE	Update TI PD controller circuit follow Mirama	Update UTS from W25Q80BLZPIG_WSON8 to W25Q80DVSSIQ_S08,Delete RT166,Change net VCC3V3_TBTA_LDO to VCC3V3_FLASH. Change net VCC3V3_SX_SYS to +3VA_TBT. Add RT198 to PWR_SRC_ILIMIT.Swap UT4.B2/C2 net. Update RT165 from 1206 to 0805, RT167,RT168, RT169,RT170,RT171,RT179,RT186,RT187,RT188,RT189,RT192,RT192,RT192,RT196,RT197 from 0402 to 0201. Add RT200,RT201 to net UPD_SMBDAT/UPD_SMBCLK"	X01
7	18	EC	2014/12/15	EE	Update Board ID for EC	Update RE67 to 62K	X01
8	18	PM	2014/12/15	EE	modify for support deep sleep function	De-pop RH506	X01
9	18	DDR	2014/12/15	EE	change Power rail for correct design	Change RH525 power rail from +3VALW to +3VS	X01
10	18	SPK	2014/12/15	EE	Add pull high resistor for MB side	Add RH572 to +3VS for SPK_DET#	X01
11	18	GPIO	2014/12/15	EE	Change GPIO for sync common GPIO table	Change net DGPU_PWR_EN from GPP_D13 to GPP_D12	X01
12	18	PD	2014/12/15	EE	Pin swap for DFB review	pin swap DT4,DT9	X01
13	18	PCH	2014/12/15	EE	Add Capacitor for follow Schematic check list	Add CH200 to +3V_PCH (Close to UH2.BA15)	X01
14	18	DIS	2014/12/15	EE	Add pull high resistor by vendor request	Add RPH34 replace to RV520,RV521,RV522 and add net THERMAL_ALERT#.	X01
15	18	SPI	2014/12/15	EE	Follow CRB XDP design	Add RH574,RH575 for SPI to XDP connector	X01
16	18	VDDQC	2014/12/16	EE	Follow CRB boardfile	POP RH473	X01
17	18	DEBUG	2014/12/16	EE	Add Debug signal by EC request	Change net BID_BC to GPP_C15, Add Net UARTT0_TX from GPP_C9 to JDEG1.pin 9	X01
18	18	DEBUG	2014/12/16	EE	Modify Debug UART from closed Chassis to Open Chassis	Delet UI6,RI29.Add JUART for UART2_TXD/UART2_RXD connect.	X01
19	18	SCI	2014/12/16	EE	Change PU resistor follow Miramar	RH383 change from 100K to 10K	X01
20	18	HOLE	2014/12/16	EE	Add 2 PAD for ME NUT	Add H50, H51	X01
21	18	EC	2014/12/16	EE	Add series resistor follow CRB	Add RE111 43K series SIO_SLP_SUS#	X01
22	18	PCH	2014/12/16	EE	Change BOM to follow CRB	Change RH88 from 10K to 47K, De-POP RE33.	X01
23	18	EC	2014/12/17	EE	Modify GPIO for follow GPIO MAP by Dell	Add RE112 and Connect net BID_DIS to UE3.A10, swap Net BAT1_LED#(UE3.B1=>UE3.A40)/BAT2_LED#(UE3.A55=>UE3.B43)/PCH_PCIE_WAKE#(UE3.A40=>UE3.B46)/ME_FWP_EC(UE3.B46=>UE3.B1)/USB_PWR_SHR_LFT_EN#(UE3.B43=>UE3.A55)	X01
24	18	EC	2014/12/17	EE	Update BOM for design change	de-POP RE27, RE63, POP RH453	X01
25	18	NGFF	2014/12/17	EE	Update NGFF from Key E. to Key A.	Change JNGFF1 to CONCR_213AAAA12FA	
26	18	PCH	2014/12/17	EE	Change array resistor to resistor for routing	Change RP21 to RH576,RH577,RH578,RH579, Add RE113,RE114,RE115 for UE1.	
27	18	USB	2014/12/18	EE	Change net name by EC request	USB_PWR_SHR_VBUS_LFT_EN -> USB_PWR_SHR_VBUS_EN_L, USB_PWR_SHR_VBUS_RHT_EN1 -> USB_PWR_SHR_VBUS_EN_R, USB_PWR_SHR_LFT_EN# -> USB_PWR_SHR_EN_L#, USB_PWR_SHR_RHT_EN1# -> USB_PWR_SHR_EN_R#, USB2_DET_EC# -> USB_DET_EC_L#, USB1_DET_EC# -> USB_DET_EC_R#	
28	18	TS	2014/12/18	EE	Update Touch Screen Connector by ME request	Update JTS to ACES_50208-00601-P01	
29	18	USB	2014/12/18	EE	Add Pull down resistor for USB2.0	Add RH580,RH581 to UH2.AD10,UH2.AG2 to GND	
30	18	AR	2014/12/19	EE	Reserve test point for Alpine Ridge	Add T199,T200,T201	
31	18	PD	2014/12/22	EE	Delete common mode chok & ESD for vendor feedback	Delete LT10,DT5	
32	18	EC	2014/12/22	EE	Delete I2C signal from EC to Codec.	Delete QE14	
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34							
35							
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